RTL8305SB -Ver. D

SINGLE-CHIP 5-PORT 10/100MBPS SWITCH CONTROLLER WITH DUAL MII INTERFACES

DATASHEET

Rev. 1.2
10 June 2003
Track ID: JATR-1076-21

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USING THIS DOCUMENT

This document is intended for use by the software engineer when programming for Realtek RTL8305SB Ver.D controller chips. Information pertaining to the hardware design of products using these chips is contained in a separate document.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2003/01/30	First release.
1.1	2003/02/12	Modify VLAN feature description.
		Add power consumption feature.
		Enhance MII/SNI/SMI timing specification.
1.2	2003/06/10	Change crystal and oscillator description.
		Change VDDAL to RVDD throughout the document.
		Add TVDD, AVDD, MVDD, and RVDD AC characteristics description.
		Add AC characteristics of MAC/PHY mode MII when DISINVERTER is pulled low.

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1. General Description

The RTL8305SB Ver.D is a 5-port Fast Ethernet switch controller that integrates memory, five MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip. All ports support 100Base-FX, which shares pins (TX+-/RX+-) with UTP ports and needs no SD+/- pins, a development using Realtek proprietary technology. To compensate for the lack of auto-negotiation in 100Base-FX applications, the RTL8305SB Ver.D can be forced into 100Base-FX half or full duplex mode, and can enable or disable flow control in fiber mode.

The five ports are separated into 3 groups (GroupX/GroupY/Port4) for flexible port configuration using strapping pins upon reset. The SetGroup pin is used to select port members in GroupX and GroupY. When the port members have been determined, you may use a mode selection pin (GxMode/Gymode/P4Mode[1:0]) to select operating interfaces such as 10/100Base-TX, 100Base-FX. Each group has 4 pins for selecting initial port status (ANEG/Force, 100/10, Full/Half, Enable/Disable Flow Control) upon reset. Upon reset, in addition to using strapping pins, the RTL8305SB Ver.D also can be configured with an EEPROM or read/write operation by a CPU through the MDC/MDIO interface.

The fifth port (port4) supports an external MAC and an external PHY interface. The external MAC interface can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with a routing engine, HomePNA, or VDSL transceiver. The external PHY interface can be set to PHY mode MII in the digital interface, and UTP or fiber in the differential interface. In order to provide diagnostics in complex network systems, the RTL8305SB Ver.D also features a loopback function in each port for a variable CPU system.

The RTL8305SB Ver.D contains a 1K entry address look-up table and supports a 16-entry CAM to avoid hash collisions and to maintain forwarding performance. The RTL8305SB Ver.D supports IEEE 802.3x full duplex flow control and back-pressure half duplex flow control. A broadcast storm filtering function is provided to filter unusual broadcast storm issues and an intelligent switch engine prevents Head-Of -Line blocking problems.

The RTL8305SB Ver.D supports five VLAN groups. These can be configured as port-based VLANs and/or 802.1Q tag-based VLANs. Two ingress filtering and egress filtering options provide flexible VLAN configuration:

- Ingress filtering option 1: The Acceptable Frame Type of the Ingress Process can be set to “Admit All” or “Admit All Tagged”.
- Ingress filtering option 2: Frames associated with a VLAN for which that port is not in the member set can be “Admit” or “Discard”.
- Egress filtering option 1: “Forward” or “Discard” ARP broadcast frames.
- Egress filtering option 2: “Forward” or “Discard” Leaky VLAN frames.

The RTL8305SB Ver.D supports several types of QoS functions with two-level priority queues to improve multimedia or real-time networking applications. The QoS functions are based on:

- Port-based priority.
- 802.1Q VLAN priority tag.
- The TOS/DS (DiffServ) field of TCP/IP.

In order to avoid the flow control function effecting the quality of high priority frames, the RTL8305SB Ver.D supports intelligent flow control for high priority frames by setting DisFCAutoOff to automatically turn off flow control for 1~2 seconds whenever a congested port receives high priority frames. When the QoS function is enabled, a VLAN tag can be inserted or removed at the output port. The RTL8305SB Ver.D will insert a VLAN priority-tag (VID=0x000) for untagged frames or remove the tag for all tagged frames. The RTL8305SB Ver.D also supports a special insert VLAN tag function to separate traffic from WAN and LAN sides in Router and Gateway applications.

Maximum packet length can be 1536 or 1552 bytes according to the initial configuration (strapping upon reset). The filtering function is supported for the 802.1D specified reserved group MAC addresses (01-80-C2-00-00-03 to 01-80-C2-00-00-0F).

The RTL8305SB Ver.D provides flexible LED functions for diagnostics, which include: 1) Four combinations of link, activity, speed, duplex and collision which are designed for convenient LED displays, such as bi-color LEDs; 2) Reset blinking; 3) Blinking time selection. The RTL8305SB Ver.D also provides a loop detection function and alarm, for network existence notification, with an output pin which can be designed as a visual LED or a status input pin for a CPU.

The RTL8305SB Ver.D implements power saving mode on a per port basis. Each port automatically enters power saving mode 10 seconds after the cable is disconnected from it. The RTL8305SB Ver.D also implements a power-down mode on a per port basis. Users can set MII Reg.0.11 to force the corresponding port to enter power-down mode, which disables all transmit/receive functions except the SMI (MDC/MDIO management interface).

Each physical layer channel of the RTL8305SB Ver.D consists of a 4B5B encoder/decoder, a Manchester encoder/decoder, a scrambler/descrambler, a transmit output driver, output wave shaping filters, a digital adaptive equalizer, a PLL circuit, and a DC restoration circuit for clock/data recovery. Friendly crossover auto detection and correction functions are also supported for easy cable connection.

The integrated chip benefits from low power consumption, advanced functions with flexible configuration for 5-port SOHO switch, Home Gateway, xDSL/Cable router, and other IA applications.

2. Features

- 5-port integrated switch controller with memory and transceiver for 10Base-T and 100Base-TX with:
  - 5-port 10/100M UTP or
  - 4-port 10/100M UTP + 1-port MII/SNI
  - 4-port 10/100M UTP + 1-port MAC MII/SNI + 1-port PHY MII
- Supports the fifth port MAC circuit as PHY mode MII, SNI for router applications, and MAC mode MII for HomePNA or VDSL solutions
- Supports the fifth port PHY circuit as PHY mode MII for router and Gateway applications
- All ports support 100Base-FX with optional flow control enable/disable and full/half duplex setting
- Non-blocking wire-speed reception and transmission and non-head-of-line-blocking forwarding
- Fully compliant with IEEE 802.3/802.3u auto-negotiation function
- Built-in high efficiency 512Kbits SRAM for packet buffer and 1K-entry look-up table, and 16-entry CAM
- Supports broadcast storm filtering function
- Supports IEEE 802.3x full duplex flow control and back pressure half duplex flow control
- Supports SMI (Serial Management Interface: MDC/MDIO) for programming and diagnostics
- Supports loop detection function with one LED to indicate the existence of loop
- Supports loopback function for diagnosis
- Supports up to five VLAN groups
- Port-based VLAN function
- 802.1Q tag VLAN forwarding
- ARP VLAN for broadcast packets
- Leaky VLAN for unicast packets
- VLAN priority tag Insert/Remove function
- Supports QoS function on each port:
  - QoS based on: (1) Port-based (2) VLAN tag (3) TCP/IP header's TOS/DS
  - Supports two-level priority queues
  - Weighted round robin service
- Supports special VLAN tag Insert function to separate WAN traffic from LAN traffic
- Supports special VLAN tag Insert function to separate WAN traffic from LAN traffic
- Optional 1536 or 1552 byte maximum packet length
- Supports reserved control frames (DID= 0180C2000003~0180C200000F) filtering function
- Flexible LED indicators for link, activity, speed, full/half duplex and collision
- LEDs blink upon reset for LED diagnostics
- Supports two Power Reduction methods:
  - Power saving mode via cable detection
  - Power down mode (via PHY register 0.11)
- Robust baseline wander correction for improved 100Base-TX performance
- Robust baseline wander correction for improved 100Base-TX performance
- Optional Crossover Detection and Auto Correction function
- Physical layer port Polarity Detection and Correction function
- Optional EEPROM interface for configuration
- Low power consumption (1.2 Watts max.)
- 25MHz crystal or 3.3V/2.5V OSC input
- Single 3.3V power input can be transformed to 2.5V via a low-cost external BJT transistor
- 0.25 μm, CMOS technology, 3.3V/2.5V with 3.3V input tolerant, 128 pin PQFP package

3. Block Diagram

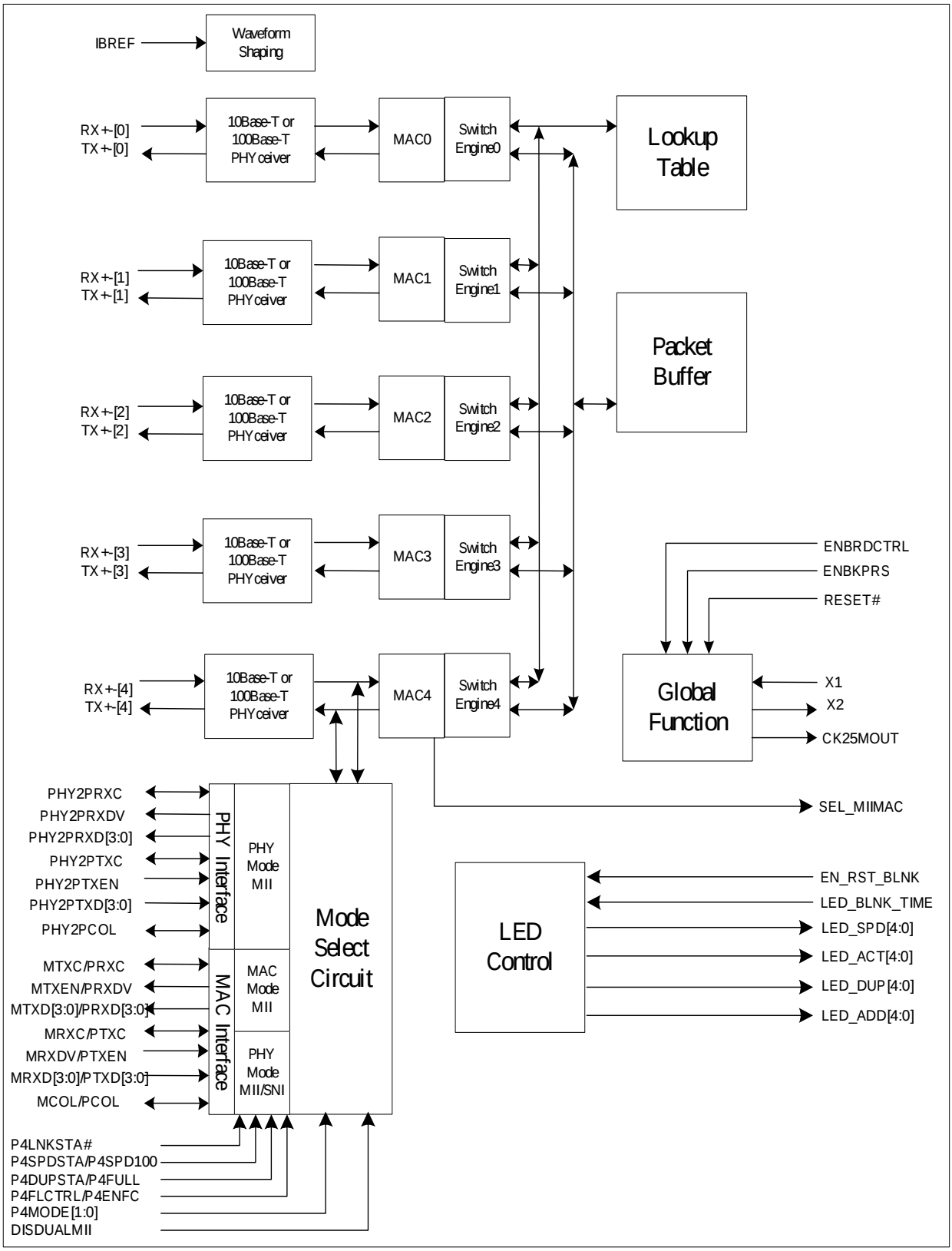


Figure 1. Block Diagram

4. Pin Assignments

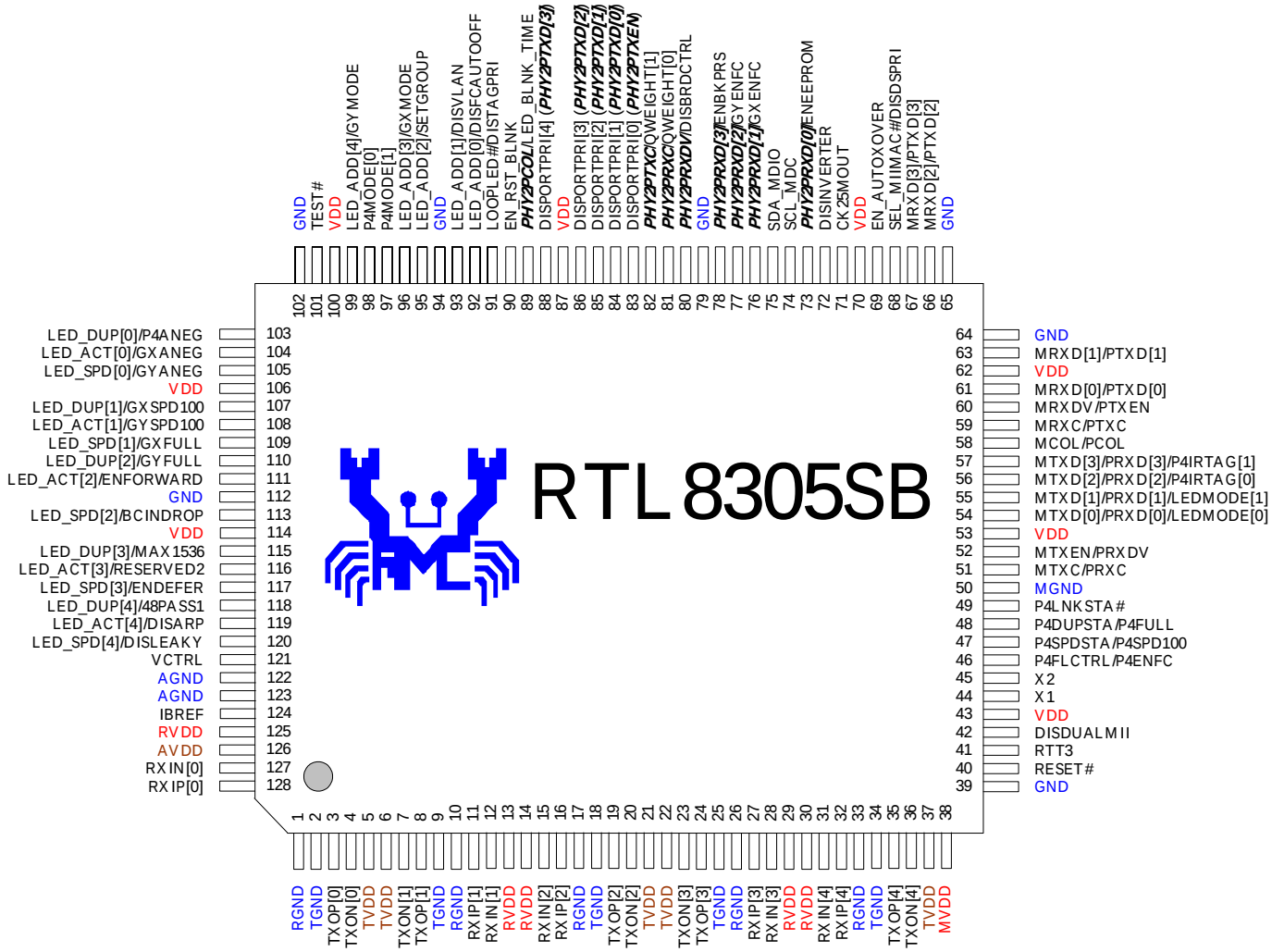


Figure 2. RTL8305SB Ver.D Pin Assignments

Note: When DISDUALMII=1, the function of pins 83~88 follows the names before the parenthesis "( )". When DISDUALMII=0, pin names in parenthesis "( )"will become functional and original pin functions will not apply.

"Type" codes used in the following tables: 'A' stands for analog; 'D' stands for digital, 'I' stands for input; 'O' stands for output.
Note2: When DISDUALMII=1, the function of pins 83~88 follows the names before the parenthesis "( )". When DISDUALMII=0, pin names in parenthesis "( )"will become functional and original pin functions will not apply.

Table 1. Pin Assignments

Name	Pin No.	Type	Name	Pin No.	Type
RGND	1	AGND	GND	65	DGND
TGND	2	AGND	MRXD[2]/PTXD[2]	66	I
TXOP[0]	3	AO	MRXD[3]/PTXD[3]	67	I
TXON[0]	4	AO	SEL_MIIMAC#/DISDSPRI	68	I/O
TVDD	5	AVDD	EN_AUTOXOVER	69	I
TVDD	6	AVDD	VDD	70	DVDD
TXON[1]	7	AO	CK25MOUT	71	O
TXOP[1]	8	AO	DISINVERTER	72	I/O
TGND	9	AGND	PHY2PRXD[0]/ENEEPROM	73	I
RGND	10	AGND	SCL_MDC	74	I/O
RXIP[1]	11	AI	SDA_MDIO	75	I/O
RXIN[1]	12	AI	PHY2PRXD[1]/GXENFC	76	I
RVDD	13	AVDD	PHY2PRXD[2]/GYENFC	77	I
RVDD	14	AVDD	PHY2PRXD[3]/ENBKPRS	78	I
RXIN[2]	15	AI	GND	79	DGND
RXIP[2]	16	AI	PHY2PRXDV/DISBRDCTRL	80	I
RGND	17	AGND	PHY2PRXC/QWEIGHT[0]	81	I
TGND	18	AGND	PHY2PTXC/QWEIGHT[1]	82	I
TXOP[2]	19	AO	DISPORTPRI[0] (**PHY2PTXEN**)	83	I
TXON[2]	20	AO	DISPORTPRI[1] (**PHY2PTXD[0]**)	84	I
TVDD	21	AVDD	DISPORTPRI[2] (**PHY2PTXD[1]**)	85	I
TVDD	22	AVDD	DISPORTPRI[3] (**PHY2PTXD[2]**)	86	I
TXON[3]	23	AO	VDD	87	DVDD
TXOP[3]	24	AO	DISPORTPRI[4] (**PHY2PTXD[3]**)	88	I
TGND	25	AGND	PHY2PCOL/LED_BLNK_TIME	89	I
RGND	26	AGND	EN_RST_BLNK	90	I
RXIP[3]	27	AI	LOOPLED#/DISTAGPRI	91	I/O
RXIN[3]	28	AI	LED_ADD[0]/DISFCAUTOOFF	92	I/O
RVDD	29	AVDD	LED_ADD[1]/DISVLAN	93	I/O
RVDD	30	AVDD	GND	94	DGND
RXIN[4]	31	AI	LED_ADD[2]/SETGROUP	95	I/O
RXIP[4]	32	AI	LED_ADD[3]/GXMODE	96	I/O
RGND	33	AGND	P4MODE[1]	97	I
TGND	34	AGND	P4MODE[0]	98	I
TXOP[4]	35	AO	LED_ADD[4]/GYMODE	99	I/O
TXON[4]	36	AO	VDD	100	DVDD
TVDD	37	AVDD	TEST#	101	I/O
MVDD	38	DVDD	GND	102	DGND
GND	39	DGND	LED_DUP[0]/P4ANEG	103	I/O
RESET#	40	I	LED_ACT[0]/GXANEG	104	I/O
RTT3	41	O	LED_SPD[0]/GYANEG	105	I/O
DISDUALMII	42	I/O	VDD	106	DVDD
VDD	43	DVDD	LED_DUP[1]/GXSPD100	107	I/O
X1	44	I	LED_ACT[1]/GYSPD100	108	I/O
X2	45	O	LED_SPD[1]/GXFULL	109	I/O
P4FLCTRL/P4ENFC	46	I	LED_DUP[2]/GYFULL	110	I/O
P4SPDSTA/P4SPD100	47	I	LED_ACT[2]/ENFORWARD	111	I/O
P4DUPSTA/P4FULL	48	I	GND	112	GND
P4LNKSTA#	49	I	LED_SPD[2]/BCINDROP	113	I/O
MGND	50	DGND	VDD	114	DVDD
MTXC/PRXC	51	I/O	LED_DUP[3]/MAX1536	115	I/O
MTXEN/PRXDV	52	O	LED_ACT[3]/RESERVED2	116	I/O
VDD	53	DVDD	LED_SPD[3],/ENDEFER	117	I/O
MTXD[0]/PRXD[0]/LEDMODE[0]	54	I/O	LED_DUP[4]/48PASS1	118	I/O
MTXD[1]/PRXD[1]/LEDMODE[1]	55	I/O	LED_ACT[4]/DISARP	119	I/O
MTXD[2]/PRXD[2]/P4IRTAG[0]	56	I/O	LED_SPD[4]/DISLEAKY	120	I/O
MTXD[3]/PRXD[3]/P4IRTAG[1]	57	I/O	VCTRL	121	O
MCOL/PCOL	58	I/O	AGND	122	AGND
MRXC/PTXC	59	I/O	AGND	123	AGND
MRXDV/PTXEN	60	I	IBREF	124	A
MRXD[0]/PTXD[0]	61	I	RVDD	125	AVDD
VDD	62	DVDD	AVDD	126	AVDD
MRXD[1]/PTXD[1]	63	I	RXIN[0]	127	AI
GND	64	DGND	RXIP[0]	128	AI

5. Pin Descriptions

"Type" codes used in the following tables: 'A' stands for analog; 'D' stands for digital, 'I' stands for input; 'O' stands for output.

Upon reset: defined as a short time after the end of a hardware reset. **After reset:** defined as the time after the specified "Upon Reset" time.

5.1. Media Connection Pins

Table 2. Media Connection Pins

Pin Name	Pin No.	Type	Description	Default
RXIP[4:0] RXIN[4:0]	11,12,15, 16,27,28, 31,32 127,128	AI	**Differential Receive Data Input:** Shared by 100Base-TX, 10Base-T, and 100Base-FX. UTP or FX depends on pin GxMode/GyMode/P4Mode[1:0].	
TXOP[4:0] TXON[4:0]	3,4 7,8 19,20 23,24 35,36	AO	**Differential Transmit Data Output:** Shared by 100Base-TX, 10Base-T, and 100Base-FX. UTP or FX depends on pin GxMode/GyMode/P4Mode[1:0].	

5.2. Configuration Pins

Table 3. Configuration Pins

Pin Name	Pin No.	Type	Description	Default
DISINVERTER	72	I	**Disable PHY Mode MII/SNI PRXC Timing of Port4 MAC circuit:** This pin disables or enables the internal inverter to adjust the PRXC timing in PHY mode MII/SNI of the port4 MAC circuit. 1: Disable 0: Enable When enabled, and the MAC circuit of port4 is configured as PHY mode MII, the PRXC outputs through an internal inverter to adjust the timing between PRXC and PRXD/PRXDV.	1
EN_RST_BLNK	90	I	**Enable Reset Blink:** This pin enables blinking of the LEDs upon reset for diagnosis purposes. 1: Enable reset LED blinking 0: Disable reset LED blinking	1

5.3. Port4 External MAC Interface Pins

The external device must be 2.5V compatible as the digital output of the RTL8305SB Ver.D is 2.5V. The input and input/output pins listed below do not have internal pull-high resistors for connecting to external devices. External pull-high resistors are recommended if reduced power consumption is desired.

Tip: Connect the input of Port4 to the output of the external device.

Table 4. Port4 External MAC Interface Pins

Pin Name	Pin No.	Type	Description	Default
Port4 Configuration Pin Definitions				
DISDUALMII	42	I/O	**Disable Dual MII Interface Function:** This pin disables or enables the Dual MII interface function of port4. 1: Disable 0: Enable When enabled, the MAC circuit of port4 can be set as MAC mode MII, PHY mode MII, or PHY mode SNI. The PHY circuit of port4 is set as PHY mode MII. The PHY circuit of port4 can optionally be set as UTP or fiber mode according to the P4MOD[1:0] configuration.	1
P4MODE[1:0]	97, 98	I	**When DISDUALMII=1, Select Port4 Operating Mode:** 11: UTP/MAC mode MII 10: 100Base-FX mode 01: PHY mode MII 00: PHY mode SNI **When DISDUALMII=0,** **I. Select Port4 Dual MII Operating Mode:** Port4 MAC Circuit operating mode: 11: MAC mode MII 10: MAC mode MII 01: PHY mode MII 00: PHY mode SNI **II. Port4 PHY Circuit Operating Mode (only PHY mode MII):** 11: 100Base-T Full Duplex UTP (only NWay with all abilities)* 10: 100Base-FX mode (only Force 100Mbps Full Duplex)** 01: 100Base-T UTP Full Duplex (only NWay with all abilities)* 00: 100Base-T UTP Full Duplex (only NWay with all abilities)* *These pins have internal 75k Ohm pull-high resistors.* **: NWay ability with Reg.4.10, Reg.4.8~5 are all 1.* ***: Reg.0.13 and Reg.0.8 are all 1.*	11

Pin Name	Pin No.	Type	Description	Default
P4LNKSTA#	49	I	**Port4 Link Status for MAC:** When the PHY part of Port4 is not used, this pin determines the link status of the Port4 MAC in real time. That is, the real-time link status of MII MAC/MII PHY/SNI PHY only. This pin is low active. 1: No Link. 0: Link When P4MODE[1:0]=11 and DISDUALMII=1 (UTP/MAC mode MII), this pin determines the link status of MAC mode MII (only) in real time. The link status of UTP mode is provided by the internal PHY in real time. If both UTP and MII port are linked OK, UTP has higher priority. When P4MODE[1:0]=11 and DISDUALMII=0 (MAC mode MII) this pin determines the link status of MAC mode MII (only) in real time. When P4MODE[1:0]=10 (100Base-FX mode), this pin does nothing. The internal PHY will provide the link status to the MAC in real time. When P4MODE[1:0]=01 (PHY mode MII), this pin determines the link status of Port4 in real time. When P4MODE[1:0]=00 (PHY mode SNI), this pin determines the link status of Port4 in real time. This pin should be left floating in UTP or FX mode, and pulled down in the other three modes. *When DISDUALMII=1 and MAC mode MII/ PHY mode MII/ PHY mode SNI, configuration of this pin sets the link status of PHY 4 MII register 1.2.* *When DISDUALMII=0 and MAC mode MII/ PHY mode MII/ PHY mode SNI, configuration of this pin sets the link status of PHY 5 MII register 1.2.*	1
P4DUPSTA/ P4FULL	48	I	**Port4 Duplex Status:** Port4 initial configuration pin for duplex upon reset for PHY in UTP or FX mode, and Duplex Status for MAC of other modes in real time after reset. 1: Full duplex 0: Half duplex When P4MODE[1:0]=11 (UTP/MAC mode MII), this pin provides the initial duplex configuration for the PHY part upon reset (UTP) then determines the duplex status of MAC mode MII in real time after reset. The duplex status of the PHY part (UTP) is provided by the internal PHY in real time after reset. When P4MODE[1:0]=10 (100Base-FX mode), this pin provides the initial register duplex configuration of the PHY part upon reset (FX). The duplex status of the PHY part (FX) is provided by the internal PHY in real time after reset. When P4MODE[1:0]=01 (PHY mode MII), this pin determines the duplex status of Port4 in real time after reset. When P4MODE[1:0]=00 (PHY mode SNI), this pin determines the duplex status of Port4 in real time after reset. In order to provide full duplex as the default value for the PHY, this pin is set as high active. In 100Base-FX/ MAC mode MII/ PHY mode MII/ PHY mode SNI, the configuration of this pin after reset will not set the link status of the internal register. The link status depends on the external PHY or MAC.	1

Pin Name	Pin No.	Type	Description	Default
P4SPDSTA/ P4SPD100	47	I	**Port4 Speed Status:** Port4 initial configuration pin for Speed upon reset for PHY of UTP mode only, and Speed Status for MAC of other modes in real time after reset. 1: 100Mbps 0: 10Mbps When P4MODE[1:0]=11 (UTP/MAC mode MII), this pin provides the initial configuration of speed for the PHY part upon reset (UTP) then determines the speed status of MAC mode MII in real time after reset. The speed status of the PHY part (UTP) is provided by the internal PHY in real time after reset. When P4MODE[1:0]=10 (100Base-FX mode), speed is dedicated to 100M and this pin does nothing and should be left floating. When P4MODE[1:0]=01 (PHY mode MII), this pin determines the speed status of Port4 in real time after reset. When P4MODE[1:0]=00 (PHY mode SNI), speed is dedicated to 10MHz clock rate. This pin should be pulled down. For the application listed below, this pin should be left floating: For P4MODE[1:0]=10 (100Base-FX mode). For the application listed below, this pin should be pulled down: For PHY mode SNI, speed is dedicated to 10MHz clock rate. In order to provide 100M as the default value for PHY, this pin is set as high active.	1
P4FLCTRL/ P4EnFC	46	I	**Port4 Flow Control:** Port4 initial configuration pin for Flow Control upon reset for PHY of UTP and FX mode. Real time Flow Control Status for MAC in other modes after reset. 1=Enable Flow Control ability. 0=Disable Flow Control ability. When P4MODE[1:0]=11 (UTP/MAC mode MII), this pin provides the initial configuration of flow control for the PHY part upon reset (UTP) then determines the flow control status of MAC mode MII in real time after reset. The flow control status of the PHY part (UTP) is provided by the internal PHY in real time after reset. When P4MODE[1:0]=10 (100Base-FX mode), this pin provides the initial configuration of flow control for the PHY part upon reset (FX). When P4MODE[1:0]=01 (PHY mode MII), this pin determines the flow control ability of Port4 in real time after reset. When P4MODE[1:0]=00 (PHY mode SNI), flow control should be disabled. This pin must be pulled down. In order to enable flow control ability for the PHY, this pin is set as high active.	1
SEL_MIIMAC#/ DisDSPri	68	I/O	**Output after reset = SEL_MIIMAC# used for LED:** When P4MODE[1:0]=11 and DISDUALMII=1, this pin indicates whether the UTP path or the MII MAC path is selected. Otherwise, this pin has no function. LED status is represented as active-low or high depending on input strapping. => If Input=1: Output 0= MII MAC port is selected. 1= UTP is selected. => If Input=0: Output 1= MII MAC port is selected. 0= UTP is selected. When P4MODE[1:0]=11, the RTL8305SB Ver.D supports UTP/MII MAC auto-detection function via the link status of Port4 UTP and the pin P4LNKSTA# setting. UTP has higher priority over MAC mode MII. **Input upon reset = DisDSPri. Disable Differentiated Service Priority:** 1: Disable DS priority 0: Enable DS priority	1

Table 5. Port4 MAC Circuit Interface Pin Definitions

Pin Name	Pin No.	Type	Description	Default
Port4 MAC Circuit Interface Pin Definitions				
MRXD[3:0]/ PTXD[3:0]	67, 66, 63, 61	I	For MAC mode MII, these pins are MRXD[3:0], MII receive data nibble. For PHY mode MII, these pins are PTXD[3:0], MII transmit data nibble. For PHY mode SNI, PTXD[0] is serial transmit data. Because these pins can be connected to 2.5V or 3.3V devices, these pins have no internal pull-high resistor.	
MRXDV/PTXEN	60	I	For MAC mode MII, this pin represents MRXDV, MII receive data valid. For PHY mode MII, this pin represents PTXEN, MII transmit enable. For PHY mode SNI, this pin represents PTXEN, transmit enable. Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor.	
MRXC/PTXC	59	I/O	For MAC mode MII, this is a receive clock (MRXC acts as input). For PHY mode MII/PHY mode SNI, it is a transmit clock (PTXC acts as output). Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor.	
MCOL/PCOL	58	I/O	For MAC mode MII, this pin represents MCOL collision (acts as input) For PHY mode MII/PHY mode SNI, this pin represents PCOL collision (acts as output). Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor.	
MTXD[3]/ PRXD[3]/ P4IRTag[1] MTXD[2]/ PRXD[2]/ P4IRTag[0]	57 56	I/O	**Output after reset:** For MAC mode MII (P4Mode[1:0]=11), these pins are MTXD[3:0], MII transmit data of MAC. For PHY mode MII (P4Mode[1:0]=01), these pins are PRXD[3:0], MII receive data of PHY. For PHY mode SNI (P4Mode[1:0]=00), PRXD[0] is SNI serial receive data. **Input upon reset: P4IRTag[1:0]** **Insert/Remove Priority Tag of Port4.** 11: Do not insert/remove Tag from Output High and Low Queue of Port4. 10: Insert Tag from Output High and Low Queue of Port4. 01: Insert Tag from Output High Queue only of Port4. 00: Remove Tag from Output High and Low Queue of Port4. These pins are used for Port4 only. Use serial EEPROM for other ports.	11

Pin Name	Pin No.	Type	Description	Default
MTXD[1]/ PRXD[1]/ LEDMode[1] MTXD[0]/ PRXD[0]/ LEDMode[0]	55 54	I/O	**Output after reset:** For MAC mode MII (P4Mode[1:0]=11), these pins are MTXD[3:0], MII transmit data of MAC. For PHY mode MII (P4Mode[1:0]=01), these pins are PRXD[3:0], MII receive data of PHY. For PHY mode SNI (P4Mode[1:0]=00), PRXD[0] is SNI serial receive data. **Input upon reset: LEDMode[1:0]** Each port has four LED indicator pins. Each pin has different indicator meanings set by pins, LEDMode[1:0]. LEDMode[1:0]=11 : Speed + Link/Act + Duplex/Col + Link/Act/Spd. LEDMode[1:0]=10 : Speed + Act + Duplex/Col + Bi-color Link/Active. LEDMode[1:0]=01 : Speed + RxAct + TxAct + Link. LEDMode[1:0]=00 : Speed + Link/Act + Col + Duplex. All LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status. Link/Act/Spd: Link, Activity, and Speed Indicator. On for link established. Blinking every 43ms when the corresponding port is transmitting or receiving at 100Mbps. Blinking every 120ms when the port is transmitting or receiving at 10Mbps.	11
MTXEN/PRXDV	52	O	For MAC mode MII, this pin represents MTXEN, MII transmit enable. For PHY mode MII, this pin represents PRXDV, MII received data valid. For PHY mode SNI, this pin represents PRXDV, received data valid.	1
MTXC/PRXC	51	I/O	For MAC mode MII, it is a transmit clock (MTXC acts as input). For PHY mode MII/PHY mode SNI, it is a receive clock (PRXC acts as output). Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor.	

Table 6. Port4 PHY Circuit Interface Pin Definitions

Pin Name	Pin No.	Type	Description	Default
			Port4 PHY Circuit Interface Pin Definitions	
DISPORTPRI[4] (PHY2PTXD[3])	88	I	**DISDUALMII=1, Enable Port-based priority QoS function of port4.** DisPortPri[4]: 1=Disable port4 priority. 0=Enable port4 priority. **DISDUALMII=0, PHY mode MII Transmit Data Nibble.** For PHY mode MII, this pin is PHY2PTXD[3]. DISPORTPRI[4] power on strapping is **not supported when DISDUALMII=0**. This configuration can be set from the MII register. *This pin has an internal 75k Ohm pull-high resistor.*	1
DISPORTPRI[3] (PHY2PTXD[2])	86	I	**DISDUALMII=1, Enable Port-based priority QoS function of port3.** DisPortPri[3]: 1=Disable port3 priority. 0=Enable port3 priority. **DISDUALMII=0, PHY mode MII Transmit Data Nibble.** For PHY mode MII, this pin is PHY2PTXD[2]. DISPORTPRI[3] power on strapping is **not supported when DISDUALMII=0**. This configuration can be set from the MII register. *This pin has an internal 75k Ohm pull-high resistor.*	1
DISPORTPRI[2] (PHY2PTXD[1])	85	I	**DISDUALMII=1, Enable Port-based priority QoS function of port2.** DisPortPri[2]: 1=Disable port2 priority. 0=Enable port2 priority. **DISDUALMII=0, PHY mode MII Transmit Data Nibble.** For PHY mode MII, this pin is PHY2PTXD[1]. DISPORTPRI[2] power on strapping is **not supported when DISDUALMII=0**. This configuration can be set from the MII register. *This pin has an internal 75k Ohm pull-high resistor.*	1

Pin Name	Pin No.	Type	Description	Default
DISPORTPRI[1] (PHY2PTXD[0])	84	I	**DISDUALMII=1, Enable Port-based priority QoS function of port1.** DisPortPri[1]: 1=Disable port1 priority. 0=Enable port1 priority. **DISDUALMII=0, PHY mode MII Transmit Data Nibble.** **For PHY mode MII, this pin is PHY2PTXD[0].** DISPORTPRI[1] power on strapping is **not supported when DISDUALMII=0**. This configuration can be set from the MII register. *This pin has an internal 75k Ohm pull-high resistor.*	1
DISPORTPRI[0] (PHY2PTXEN)	83	I	**DISDUALMII=1, Enable Port-based priority QoS function of port0.** DisPortPri[0]: 1=Disable port0 priority. 0=Enable port0 priority. **DISDUALMII=0, PHY mode MII Transmit Data Enable.** For PHY mode MII, this pin is PHY2PTXEN. DISPORTPRI[0] power on strapping is **not supported when DISDUALMII=0**. This configuration can be set from the MII register. *This pin has an internal 75k Ohm pull-high resistor.* *For Dual MII application, this pin should be pulled low (about 10k ohm) in external circuit.*	1
PHY2PCOL/ LED_BLNK_ TIME	89	I/O	**DISDUALMII=0, PHY mode MII PCOL.** For PHY mode MII, this pin represents PCOL collision (acts as output) **LED Blink Time:** This pin selects the blinking speed of the activity and collision LEDs. 1: On 43ms, then Off 43ms 0: On 120ms, then Off 120ms *This pin has an internal 75k Ohm pull-high resistor.* *Power on strapping is independent of DISDUALMII configuration.*	1
PHY2TXC/ QWEIGHT[1] PHY2RXC/ QWEIGHT[0]	82 81	I/O	**DISDUALMII=0, PHY mode MII Transmit/Receive Data Clock.** For PHY mode MII, this is transmit/receive data clock, PTXC/PRXC (acts as output). **Weighted round robin ratio of priority queue.** The frame service rate of High-pri queue: Low-pri queue QWEIGHT[1:0]=11: 16:1 QWEIGHT[1:0]=10: always high priority queue first QWEIGHT[1:0]=01: 8:1 QWEIGHT[1:0]=00: 4:1 *These pins have an internal 75k Ohm pull-high resistor.* *Power on strapping is independent of DISDUALMII configuration.*	11
PHY2RXD[3]/ ENBKPRS	78	I/O	**DISDUALMII=0, PHY mode MII Receive Data Nibble (acts as output).** For PHY mode MII, this pins is PHY2PRXD[3]. **Enable Back Pressure:** This pin sets back pressure in half duplex mode on all UTP ports. 1: Enable 0: Disable *This pin has an internal 75k Ohm pull-high resistor.* *Power on strapping is independent of DISDUALMII configuration.*	1

Pin Name	Pin No.	Type	Description	Default
PHY2RXD[2]/ GYENFC	77	I/O	**DISDUALMII=0, PHY mode MII Receive Data Nibble (acts as output).** For PHY mode MII, this pins is PHY2PRXD[2]. **GroupY Enable Flow Control ability:** 1: Enable Reg4.10 (NWAY Full duplex only), or "Enable Force Full pause ability of Force mode (UTP Force mode or FX mode)", or "Enable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)". 0: Disable Reg4.10 (NWAY Full duplex only), or "Disable Force Full pause ability of Force mode (UTP Force mode or FX mode)", or "Disable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)". Strap after reset for initial value of Group Y "UTP NWAY Full", or "UTP Force Full or Half mode", or "FX Full or Half mode". *This pin has an internal 75k Ohm pull-high resistor.* *Power on strapping is independent of DISDUALMII configuration.*	1
PHY2RXD[1]/ GXENFC	76	I/O	**DISDUALMII=0, PHY mode MII Receive Data Nibble (acts as output).** For PHY mode MII, this pin is PHY2PRXD[1]. **GroupX Enable Flow Control ability:** 1: Enable Reg4.10 (NWAY Full duplex only), or "Enable Force Full pause ability of Force mode (UTP Force mode or FX mode)", or "Enable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)". 0: Disable Reg4.10 (NWAY Full duplex only), or "Disable Force Full pause ability of Force mode (UTP Force mode or FX mode)", or "Disable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)". Strap after reset for initial value of Group X "UTP NWAY Full", or "UTP Force Full or Half mode", or "FX Full or Half mode". *This pin has an internal 75k Ohm pull-high resistor.* *Power on strapping is independent of DISDUALMII configuration.*	1
PHY2RXD[0]/ ENEEPROM	73	I/O	**DISDUALMII=0, PHY mode MII Receive Data Nibble (acts as output).** For PHY mode MII, this pin is PHY2PRXD[0]. **Enable EEPROM:** This pin sets the RTL8305SB to enable loading of the serial EEPROM upon reset. 1: Enable 0: Disable *This pin has an internal 75k Ohm pull-high resistor.* *Power on strapping is independent of DISDUALMII configuration.*	1
PHY2RXDV/ DISBRDCTRL	80	I/O	**DISDUALMII=0, PHY mode MII Receive Data Valid.** For PHY mode MII, this pin represents PRXDV. **Disable Broadcast Storm Control:** 1= Disable 0= Enable The RTL8305SB Ver.D will disable this function when pin DISBRDCTRL is left floating. *This pin has an internal 75k Ohm pull-high resistor.* *Power on strapping is independent of DISDUALMII configuration.*	1

5.4. Miscellaneous Pins

Table 7. Miscellaneous Pins

Pin Name	Pin No.	Type	Description	Default
X1	44	I	25MHz crystal or oscillator clock input. The clock tolerance is +-50ppm.	
X2	45	O	For crystal input, when using an oscillator, this pin should be floating.	
CK25MOUT	71	O	25MHz clock output. The source of this output is the clock from X1 and X2. This pin is used to support an extra 25M clock for an external device (for example: HomePNA PHY).	
RESET#	40	I	**Active low reset signal:** To complete the reset function, this pin must be asserted for at least 1ms. After reset, about 30ms is needed for the RTL8305SB to complete internal test functions and initialization. This pin is a Schmitt input. Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor.	
IBREF	124	A	**Control transmit output waveform Vpp:** This pin should be grounded through a 1.96KΩ resistor.	
VCTRL	121	O	**Voltage control to external regulator:** This signal controls a power PNP transistor to generate the 2.5V power supply.	
RTT3	41	O	Reserved pin for internal use. Should be left floating.	
TEST#	101	I/O	Reserved pin for internal use. Should be left floating.	1

5.5. Port LED Pins

Each port has four LED indicator pins. Each pin may have different indicator meanings as set by pins LEDMode[1:0].

All LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status.

Those pins that are dual function pins are output for LED or input for strapping. Below are LED descriptions only.

Table 8. Port LED Pins

Pin Name	Pin No.	Type	Description	Default
LED_SPD[4:0]/…	120, 117, 113, 109, 105	I/O	**Output after reset = used for 1st LED:** LEDMode[1:0]=11 -> Speed (0n=100, Off=10) LEDMode[1:0]=10 -> Speed (0n=100, Off=10) LEDMode[1:0]=01 -> Speed (0n=100, Off=10) LEDMode[1:0]=00 -> Speed (0n=100, Off=10) **Input upon reset = Refer to Table 5, page 10, pins 54 and 55.**	11111
LED_ACT[4:0]/…	119, 116, 111, 108, 104	I/O	**Output after reset = used for 2nd LED:** LEDMode[1:0]=11 -> Link/Act: (On=Link, Off=no Link, Flash=Tx or Rx activity) LEDMode[1:0]=10 -> Act: (Off=no activity, On=Tx or Rx activity) LEDMode[1:0]=01 -> RxAct: (Off=no activity, On=Rx activity) LEDMode[1:0]=00 -> Link/Act: (On=Link, Off=no Link, Flash=Tx or Rx activity) **Input upon reset = Refer to Table 5, page 10, pins 54 and 55.**	11111
LED_DUP[4:0]/…	118, 115, 110, 107, 103	I/O	**Output after reset = used for 3rd LED:** LEDMode[1:0]=11 -> Duplex/Col: (On=Full, Off=Half with no collision, Flash=Collision) LEDMode[1:0]=10 -> Duplex/Col: (On=Full, Off=Half with no collision, Flash=Collision) LEDMode[1:0]=01 -> TxAct: (Off=no activity, On=Tx activity) LEDMode[1:0]=00 -> Col: (Off=Half with no collision, On=Collide) **Input upon reset = Refer to Table 5, page 10, pins 54 and 55.**	11111

Pin Name	Pin No.	Type	Description	Default
LED_ADD[4:0]/…	99, 96, 95, 93, 92	I/O	**Output after reset = used for 4th LED:** LEDMode[1:0]=11 -> Link/Act/Spd: On for link established. Blinking every 43ms when the corresponding port is transmitting or receiving at 100Mbps. Blinking every 120ms when the port is transmitting or receiving at 10Mbps. LEDMode[1:0]=10 -> Bi-color Link/Active: polarity depends on Spd status. See Figure 23 on page 56, Figure 24 on page 56, and Table 48 on page 56. LEDMode[1:0]=01 -> Link: (On=Link, Off=no Link) LEDMode[1:0]=00 -> Duplex: (On=Full, Off=Half) **Input upon reset = Refer to Table 5, page 10, pins 54 and 55.**	11111

5.6. Power Pins

Table 9. Power Pins

Pin Name	Pin No.	Type	Description	Default
TVDD	5, 6, 21, 22, 37	P	3.3V Analog Transmit Power	
RVDD	13, 14 29, 30	P	2.5V Analog Receive Power	
AVDD	126	P	3.3V Analog Power	
RVDD	125	P	2.5V Analog Receive Power	
MVDD	38	P	2.5V Internal RAM Power	
VDD	43, 53 62, 70 87, 100 106, 114	P	2.5V Digital Power	
RGND	1, 10, 17, 26, 33	P	Analog Ground	
TGND	2, 9, 18, 25, 34	P	Analog Ground	
AGND	122, 123	P	Analog Ground	
MGND	50	P	Internal RAM GND	
GND	39, 64, 65, 79 94, 102 112	P	Digital GND	

5.7. Serial EEPROM and SMI Pins

The serial EEPROM and external device must be 2.5V compatible, as the output of the RTL8305SB is 2.5V. If the external device output is 3.3V, there will be 0.7V (3.3V–2.5V) on pull-high resistors.

Table 10. Serial EEPROM and SMI Pins

Pin Name	Pin No.	Type	Description	Default
SCL_MDC	74	I/O	**SCL or MDC:** This pin is tri state when pin RESET#=0. When pin EnEEPROM=1, this pin becomes SCL (output) to load the serial EEPROM upon reset. Then this pin changes to MDC (input) after reset. In this case, this pin should be pulled-high (2.5V) by an external resistor. When pin EnEEPROM=0, this pin is MDC (input): 0 to 25MHz clock, sourced by an external device to sample MDIO. In this case, if, and only if, this pin is floating, it needs an external pull-high (2.5V) resistor. Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor.	
SDA_MDIO	75	IO	**SDA or MDIO:** This pin is tri state when RESET#=0. When pin EnEEPROM=1, this pin becomes SDA (input/output) to load the serial EEPROM upon reset. Then this pin changes to MDIO (input/output) after reset. When pin EnEEPROM=0, this pin is MDIO (input/output). It should be pulled-high by an external resistor. Because this pin can be connected to a 2.5V or 3.3V device, this pin has no internal pull-high resistor.	

5.8. Strapping Pins

Pins that are dual function pins are outputs for LED or inputs for strapping. Below are strapping descriptions only.

Table 11. Strapping Pins

Pin Name	Pin No.	Type	Description	Default
EN_AUTO XOVER	69	I	**Enable Auto crossover function:** 1: Enable auto crossover detection. 0: Disable auto crossover detection. MDI only.	1
LoopLED# /DisTagPri	91	I/O	**Output after reset = LoopLED# used for LED:** If the Loop detection function is enabled, this pin indicates whether Network loop is detected or not. Otherwise, this pin is of no use. The LED statuses are represented as active-low or high depending on input strapping. => If Input=1: Output 0=Network loop is detected. 1=No loop. => If Input=0: Output 1=Network loop is detected. 0=No loop. **Input upon reset = Disable 802.1p VLAN Tag priority based QoS function.** 1: Disable 0: Enable	1
LED_ADD[0]/ DisFCAutoOff	92	I/O	**Output after reset = used for LED:** **Input upon reset = Disable Auto Turn Off function of Flow Control Ability.** 1: Disable 0: Enable. Enables Auto turn off of low priority queue's flow control ability for 1~2 sec whenever the port receives a VLAN-tag or TOS/DS high priority frame. The flow control ability is re-enabled when no high priority frame has been received for 1~2 seconds.	1
LED_ADD[1]/ DISVLAN	93	I/O	**Output after reset = used for LED:** **Input upon reset = Disable VLAN function.** 1: Disable VLAN 0: Enable VLAN According to the internal registers	1

Pin Name	Pin No.	Type	Description	Default
LED_ACT[2]/ EnForward	111	I/O	**Output after reset = used for LED** **Input upon reset = Enable to forward 802.1D specified reserved group MAC addresses frame.** 1: Forward reserved control frames, with DID=01-80-C2-00-00-03 to 01-80-C2-00-00-0F. 0: Filter reserved control packets, with DID=01-80-C2-00-00-03 to 01-80-C2-00-00-0F.	1
LED_SPD[2]/ BCInDrop	113	I/O	**Output after reset = used for LED** **Input upon reset = Broadcast Input Drop.** 1: Use Broadcast Input drop mechanism. 0: Use Broadcast Output drop mechanism.	1
LED_DUP[3]/ Max1536	115	I/O	**Output after reset = used for LED** **Input upon reset = Maximum Frame Length** 1: 1536 Bytes 0: 1552 Bytes	1
LED_DUP[4]/ 48pass1 LED_SPD[3]/ EnDefer LED_ACT[3]/ RESERVED2	118 117 116	I/O	**Output after reset = used for LED** **Input upon reset = Back pressure mode.** **48pass1:** 1: 48 pass 1: Allows at most 48 consecutive collisions in order to prevent repeater partition when buffer is full. 0: Continuously collides to avoid packet loss when buffer is full. **EnDefer:** 1: Enable Carrier Sense Deferring function for half duplex back pressure. 0: Disable Carrier Sense Deferring function for half duplex back pressure.	111
LED_ACT[4] /DisARP	119	I/O	**Output after reset = used for LED:** **Input upon reset = Disable ARP broadcast to all VLANs.** 1: Disables ability to broadcast ARP broadcast packets to all VLANs. 0: Enables ability to broadcast ARP broadcast packets to all VLANs. ARP broadcast frame: DID is all F.	1
LED_SPD[4]/ DisLeaky	120	I/O	**Output after reset = used for LED:** **Input upon reset = Disable Leaky VLAN.** 1: Disable forwarding of unicast frames to other VLANs. 0: Enable forwarding of unicast frames to other VLANs. Broadcast and multicast frames adhere to the VLAN configuration.	1

5.9. Port Status Strapping Pins

Pins that are dual function pins are outputs for LEDs or inputs for strapping. Below are strapping descriptions only.

Table 12. Port Status Strapping Pins

Pin Name	Pin No.	Type	Description	Default
LED_ADD[2] /SetGroup	95	I/O	**Output after reset = used for LED:** **Input upon reset = Set group of port1:** 1: Port0 is group X. Port1, 2, and 3 are group Y 0: Port0, and 1 are group X. Port2, and 3 are group Y	1
LED_ADD[3] /GxMode	96	I/O	**Output after reset = used for LED:** **Input upon reset = Group X operating mode:** 1: UTP mode 0: FX mode	1
LED_ADD[4] /GyMode	99	I/O	**Output after reset = used for LED:** **Input upon reset = Group Y operating mode:** 1: UTP mode 0: FX mode	1

Pin Name	Pin No.	Type	Description	Default
LED_DUP[0] /P4ANEG	103	I/O	**Output after reset = used for LED:** **Input upon reset = Port4 Auto-Negotiation ability:** 1: Enable auto-negotiation (NWAY mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0.12 of Port4. Strap after reset for initial value of Port4 UTP mode only. This pin is not used for Port4 FX, MAC mode MII, PHY mode MII, and PHY mode SNI.	1
LED_ACT[0] /GxANEG	104	I/O	**Output after reset = used for LED:** **Input upon reset = GroupX Auto-Negotiation ability:** 1: Enable auto-negotiation (NWAY mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0.12 of Group X. Strap after reset for initial value of UTP mode only. This pin is not used for FX.	1
LED_SPD[0] /GyANEG	105	I/O	**Output after reset = used for LED:** **Input upon reset = GroupY Auto-Negotiation ability:** 1: Enable auto-negotiation (NWAY mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0.12 of Group Y. Strap after reset for initial value of UTP mode only. This pin is not used for FX.	1
LED_DUP[1] /GxSpd100	107	I/O	**Output after reset = used for LED:** **Input upon reset = GroupX 10Base-T/100Base-TX ability:** GxSpd100=1, GxFull=1 => MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1 GxSpd100=1, GxFull=0 => MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1 GxSpd100=0, GxFull=1; => MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1 GxSpd100=0, GxFull=0; => MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 Upon reset, this pin sets Reg.0.13. In addition, upon reset, this pin and GxFull also sets Reg.4.8/4.7/4.6/4.5. Strap after reset for initial value of Group X UTP mode only. This pin is not used for FX.	1
LED_ACT[1] /GySpd100	108	I/O	**Output after reset = used for LED:** **Input upon reset = GroupY 10Base-T/100Base-TX ability:** GySpd100=1, GyFull=1 => MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1 GySpd100=1, GyFull=0 => MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1 GySpd100=0, GyFull=1; => MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1 GySpd100=0, GyFull=0; => MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 Upon reset, this pin sets Reg.0.13. In addition, upon reset, this pin and GyFull also sets Reg.4.8/4.7/4.6/4.5. Strap after reset for initial value of Group Y UTP mode only. This pin is not used for FX.	1
LED_SPD[1] /GxFull	109	I/O	**Output after reset = used for LED:** **Input upon reset = GroupX Full Duplex ability:** Upon reset, this pin sets the default value of Reg.0.8. In addition, on reset, this pin also sets NWay full-duplex ability on Reg.4.8 and Reg.4.6. Strap after reset for initial value of Group X UTP or FX mode. FX can be Force 100 Full or Force 100 Half.	1
LED_DUP[2] /GyFull	110	I/O	**Output after reset = used for LED:** **Input upon reset = GroupY Full Duplex ability:** Upon reset, this pin sets the default value of Reg.0.8. On reset, this pin also sets NWay full-duplex ability on Reg.4.8 and Reg.4.6. Strap after reset for initial value of Group Y UTP or FX mode. FX can be Force 100 Full or Force 100 Half.	1

6. Register Descriptions

Hardware Reset: pin RESET#=0 to 1. Reset all then load EEPROM and Pin registers with serial EEPROM and Pin strapping.

Soft Reset: Write bit15 of Reg16 of PHY3 as 1. Reset all except loading EEPROM and Pin Registers with serial EEPROM and Pins. After updating the EEPROM or Pin registers via SMI, the external device must do a soft reset in order to change the configuration.

In this section the following abbreviations are used:

RO: Read Only

RW: Read/Write

LL: Latch Low until clear

LH: Latch High until clear

SC: Self Clearing

Table 13. Register Descriptions

Name	Soft Reset	PHY	Register	Register Description
Port0 PHY Reg	No	0	0	Control Register
			1	Status Register
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
Port1 PHY Reg	No	1	0	Control Register
			1	Status Register
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
Port2 PHY Reg	No	2	0	Control Register
			1	Status Register
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
Port3 PHY Reg	No	3	0	Control Register
			1	Status Register
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
Port4 PHY Reg	No	4	0	Control Register
			1	Status Register
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
EEPROM Reg0	Need	0	16~22	Register for EEPROM
EEPROM Reg1	Need	1	16~31	Register for EEPROM
Pin Reg	Need	2	16	Register for configuration Pins
Pin & EEPROM Reg	Need	2	17	Register for configuration Pins and EEPROM
Port Control Reg	No	3	16	Register for Port Control
EEPROM Reg	Need	3	17~20	Register for EEPROM

6.1. PHY0 to 4: PHY Register of Each Port

Note: XXXXb means coding in binary. XXXXh means coding in hexadecimal.

6.1.1. Register0: Control Register

Table 14. Register0: Control Register

Reg.bit	Name	Description	Mode	Default
0.15	Reset	**Reset:** 1: PHY reset. This bit is self-clearing.	RW/SC	0b
0.14	Loopback (digital loopback)	**Enable Loopback:** This pin enables loopback from the MII TXD to the MII RXD and ignores all activities on the cable media. 1: Enable loopback 0: Normal operation This function is usable only when this PHY is 10Base-T full duplex or 100Base-T full duplex. The packet is forwarded from another PHY (could be 10Base-T, or 100TX, or 100FX, both full and half duplex) by the switch core and will loopback to the switch core. It could be forwarded to another port or dropped depending on the destination and source MAC address of the packet.	RW	0b
0.13	Spd_Sel	Speed Select: 1: 100Mbps 0: 10Mbps When NWay is enabled, this bit reflects the result of auto-negotiation (Read only) When NWay is disabled, this bit can be set through SMI. (Read/Write) When 100FX mode is enabled, this bit =1 (Read only)	RW	From pin
0.12	Auto Negotiation Enable	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write) When 100FX mode is enabled, this bit =0 (Read only) 100FX must be in Force Mode. In order to avoid errors, the RTL8305SB Ver.D will ignore the action of this bit when writing Reg0.12 as 1 in 100FX mode.	RW	From pin
0.11	Power Down	1: Power down. All functions will be disabled except SMI function and internal TXC to MAC 0: Normal operation	RW	0b
0.10	Isolate	1: Electrically isolate the PHY from internal MII. The PHY is still able to response to MDC/MDIO 0: Normal operation	RW	0b
0.9	Restart Auto Negotiation	1: Restart Auto-Negotiation process 0: Normal operation	RW/SC	0b
0.8	Duplex Mode	Duplex mode: 1: Full duplex operation 0: Half duplex operation When NWay is enabled (Reg0.12=1), this bit reflects the result of auto-negotiation (Read only) When NWay is disabled (Reg0.12=0, force mode of UTP or 100FX), this bit can be set through SMI* (Read/Write). 100FX must be in Force Mode. In order to avoid errors, the RTL8305SB will ignore the action to this bit when writing Reg0.12 as 1 in 100FX mode.	RW	From pin
0.[7:0]	Reserved		RO	0b

6.1.2. Register1: Status Register

Table 15. Register1: Status Register

Reg.bit	Name	Description	Mode	Default
1.15	100Base_T4	0: No 100Base-T4 capability	RO	0b
1.14	100Base_TX_FD	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	RO	1b
1.13	100Base_TX_HD	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	RO	1b
1.12	10Base_T_FD	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	RO	1b
1.11	10Base_T_HD	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	RO	1b
1.[10:7]	Reserved		RO	00b
1.6	MF Preamble Suppression	The RTL8305SB will accept management frames with preamble suppressed. The RTL8305SB accepts management frames without preamble. Minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as defined in IEEE802.3u specs.	RO	1b
1.5	Auto-negotiate Complete	1: Auto-negotiation process completed. MII Reg.4 and 5 are valid if this bit is set 0: Auto-negotiation process not completed	RO	0b
1.4	Remote Fault	1: Remote fault condition detected 0: No remote fault When in 100FX mode, this bit means in-band signal Far-End-Fault is detected.	RO/LH	0b
1.3	Auto-Negotiation Ability	1: NWay auto-negotiation capable (permanently: 1)	RO	1b
1.2	Link Status	1: Link is established. If the link fails, this bit will be 0 until after reading this bit again 0: Link failed	RO/LL	0b
1.1	Jabber Detect	0: No Jabber detected *Note: This function is not necessary for single chip.*	RO	0b
1.0	Extended Capability	1: Extended register capable. (permanently: 1)	RO	1b

6.1.3. Register4: Auto-Negotiation Advertisement Register

Table 16. Register4: Auto-Negotiation Advertisement Register

Reg.bit	Name	Description	Mode	Default
4.15	Next Page	1: Next Page enabled 0: Next Page disabled (Permanently: 0)	RO	0b
4.14	Acknowledge	Permanently: 0	RO	0b
4.13	Remote Fault	1: Advertises that the RTL8305SB has detected a remote fault 0: No remote fault detected	RW	0b
4.[12:11]	Reserved		RO	00b
4.10	Pause	1: Advertises that the RTL8305SB has flow control capability 0: No flow control capability	RW	From pin
4.9	100Base-T4	Technology not supported (Permanently =0)	RO	0b
4.8	100Base-TX-FD	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	RW	From pin
4.7	100Base-TX	1: 100Base-TX half duplex capable. 0: Not 100Base-TX half duplex capable.	RW	From pin
4.6	10Base-T-FD	1: 10Base-TX full duplex capable. 0: Not 10Base-TX full duplex capable.	RW	From pin

Reg.bit	Name	Description	Mode	Default
4.5	10Base-T	1: 10Base-TX half duplex capable. 0: Not 10Base-TX half duplex capable.	RW	1b
4.[4:0]	Selector Field	[00001]=IEEE802.3	RW	00001b

6.1.4. Register5: Auto-Negotiation Link Partner Ability Register

Table 17. Register5: Auto-Negotiation Link Partner Ability Register

Reg.bit	Name	Description	Mode	Default
5.15	Next Page	1: Link partner desires Next Page transfer. 0: Link partner does not desire Next Page transfer.	RO	0b
5.14	Acknowledge	1: Link Partner acknowledges reception of FLP words. 0: Not acknowledged by Link Partner.	RO	0b
5.13	Remote Fault	1: Remote Fault indicated by Link Partner. 0: No remote fault indicated by Link Partner.	RO	0b
5.[12:11]	Reserved		RO	00b
5.10	Pause	1: Flow control supported by Link Partner. 0: No flow control supported by Link Partner. *Note: This bit is read only when Reg0.12=1. This bit is read/write when Reg.0.12=0 (for future use).*	RW	1b
5.9	100Base-T4	1: 100Base-T4 supported by Link Partner. 0: 100Base-T4 not supported by Link Partner.	RO	0b
5.8	100Base-TX-FD	1: 100Base-TX full duplex supported by Link Partner. 0: 100Base-TX full duplex not supported by Link Partner. For 100FX mode, this bit is set when Reg.0.8=1 or **Full =1 after link established. When NWay is disabled, this bit is set when Reg.0.13=1, and Reg.0.8=1 after link established.	RO	0b
5.7	100Base-TX	1: 100Base-TX half duplex supported by Link Partner. 0: 100Base-TX half duplex not supported by Link Partner. For 100FX mode, this bit is set when Reg.0.8=0 or **Full = 0 after link established. When NWay is disabled, this bit is set when Reg.0.13=1, and Reg.0.8=0 after link established.	RO	0b
5.6	10Base-T-FD	1: 10Base-TX full duplex supported by Link Partner. 0: 10Base-TX full duplex not supported by Link Partner. When NWay is disabled, this bit is set when Reg.0.13=0,and Reg.0.8=1 after link established.	RO	0
5.5	10Base-T	1: 10Base-TX half duplex supported by Link Partner. 0: 10Base-TX half duplex not supported by Link Partner. When NWay is disabled, this bit is set when Reg.0.13=0, and Reg.0.8=0. after link established	RO	0b
5.[4:0]	Selector Field	[00001]=IEEE 802.3	RO	00001b

6.2. PHY0: EEPROM Register0

6.2.1. Register16: EEPROM Byte0 and 1 Register

Table 18. Register16: EEPROM Byte0 and 1 Register

Reg.bit	Name	Description	Mode	Default
16.15	Internal		RW	1b
16.14	DisLoop	**Disable Loop Detection Function** 1: Disable Loop Detection function. 0: Enable Loop Detection function.	RW	1b
16.13	Internal		RW	1b
16.12	Internal		RW	1b
16.11	EnP4LED	**Enable Port4 LED** 1: Drive LED pins of port4. 0: Do not drive LED pins of port4 for special application. In UTP applications, this bit should be 1 to drive LEDs of port4.	RW	1b
16.[10:8]	Reserved		RO	111b
16.7	Internal		RW	1b
16.6	Internal		RW	1b
16.5	Internal		RW	1b
16.4	Internal		RW	1b
16.3	Internal		RW	1b
16.2	Internal		RW	1b
16.1	Internal		RW	1b
16.0	NoEEPROM	1: EEPROM does not exist (pin EnEEPROM=0. Or pin EnEEPROM=1 but no EEPROM) 0: EEPROM exists (pin EnEEPROM=1 and have EEPROM)	RO	

6.2.2. Register17: EEPROM Byte2 and 3 Register

Table 19. Register17: EEPROM Byte2 and 3 Register

Reg.bit	Name	Description	Mode	Default
17.15~ 17.10	Reserved		RO	1b
17.9	Internal	**Internal Use Only:** Should be 1	RW	1b
17.8	Internal	**Internal Use Only:** Should be 1	RW	1b
17.7~ 17.4	Reserved		RO	1111b
17.3~ 17.0	Internal	**Internal Use Only:** Should be 0000	RW	0000b

6.2.3. Register18~20: EEPROM EthernetID Register For Bytes4~9

Table 20. Register18~20: EEPROM EthernetID Register for Bytes4~9

Reg.bit	Name	Description	Mode	Default
18	EthernetID	**Device Ethernet MAC ID:** Byte4, 5 of EEPROM	RW	[7:0]= 52h [15:8]= 54h
19	EthernetID	**Device Ethernet MAC ID:** Byte6, 7 of EEPROM	RW	[7:0]= 4Ch [15:8]=83h
20	EthernetID	**Device Ethernet MAC ID:** Byte8, 9 of EEPROM	RW	[7:0]= 05h [15:8]= B0h

6.2.4. Register21: EEPROM Byte10 and 11 Register

Table 21. Register21: EEPROM Byte10 and 11 Register

Reg.bit	Name	Description	Mode	Default
21.15	Reserved		RO	1b
21.14~21.12	P3VLANIndex[2] P3VLANIndex[1] P3VLANIndex[0]	**Port3 VLAN Index:** P3VLANIndex[2:0]=0b011 means port3 uses the fourth VLAN (VLAN D)	RW	011b
21.11	Reserved		RO	1b
21.10~21.8	P2VLANIndex[2] P2VLANIndex[1] P2VLANIndex[0]	**Port2 VLAN Index:** P2VLANIndex[2:0]=0b010 means port2 uses the third VLAN (VLAN C)	RW	010b
21.7	Reserved		RO	1b
21.6~21.4	P1VLANIndex[2] P1VLANIndex[1] P1VLANIndex[0]	**Port1 VLAN Index:** P1VLANIndex[2:0]=0b001 means port1 uses the second VLAN (VLAN B)	RW	001b
21.3	Reserved		RO	1b
21.2~ 21.0	P0VLANIndex[2] P0VLANIndex[1] P0VLANIndex[0]	**Port0 VLAN Index:** P0VLANIndex[2:0] are used to assign the VLAN of port0. For example, P0VLANIndex[2:0]=0b000 means port0 uses the first VLAN (VLAN A) P0VLANIndex[0] is bit0, P0VLANIndex[1] is bit1, P0VLANIndex[2] is bit2	RW	000b

6.2.5. Register22: EEPROM Byte12 and 13 Register

Table 22. Register22: EEPROM Byte12 and 13 Register

Reg.bit	Name	Description	Mode	Default
22.15 22.14	P3IRTag[1] P3IRTag[0]	**Insert/Remove Priority Tag of Port3:** 11: Do not insert/remove Tag from Output High and Low Queue of Port3 10: Insert Tag from Output High and Low Queue of Port3 01: Insert Tag from Output High Queue only of Port3 00: Remove Tag from Output High and Low Queue of Port3	RW	11b
22.13 22.12	P2IRTag[1] P2IRTag[0]	**Insert/Remove Priority Tag of Port2:** 11: Do not insert/remove Tag from Output High and Low Queue of Port2 10: Insert Tag from Output High and Low Queue of Port2 01: Insert Tag from Output High Queue only of Port2 00: Remove Tag from Output High and Low Queue of Port2	RW	11b

Reg.bit	Name	Description	Mode	Default
22.11 22.10	P1IRTag[1] P1IRTag[0]	**Insert/Remove Priority Tag of Port1:** 11: Do not insert/remove Tag from Output High and Low Queue of Port1 10: Insert Tag from Output High and Low Queue of Port1 01: Insert Tag from Output High Queue only of Port1 00: Remove Tag from Output High and Low Queue of Port1	RW	11b
22.9 22.8	P0IRTag[1] P0IRTag[0]	**Insert/Remove Priority Tag of Port0:** 11: Do not insert/remove Tag from Output High and Low Queue of Port0 10: Insert Tag from Output High and Low Queue of Port0 01: Insert Tag from Output High Queue only of Port0 00: Remove Tag from Output High and Low Queue of Port0	RW	11b
22.7 22.6	P4IRTag[1] P4IRTag[0]	**Insert/Remove Priority Tag of Port4:** 11: Do not insert/remove Tag from Output High and Low Queue of Port4 10: Insert Tag from Output High and Low Queue of Port4 01: Insert Tag from Output High Queue only of Port4 00: Remove Tag from Output High and Low Queue of Port4	RW	11b
22.5~22.3	Reserved		RO	111b
22.2~ 22.0	P4VLANIndex[2] P4VLANIndex[1] P4VLANIndex[0]	**Port4 VLAN Index:** P4VLANIndex[2:0]=0b100 means port4 uses the fifth VLAN (VLAN E)	RW	100b

6.3. PHY1: EEPROM Register1

6.3.1. Register16~23: EEPROM (Bytes14~29) Register

Table 23. Register16~23: EEPROM (Bytes14~29) Register

Reg.bit	Name	Description	Mode	Default
16	Internal	Internal use only	RW	
17	Internal	Internal use only	RW	
18	Internal	Internal use only	RW	
19	Internal	Internal use only	RW	
20	Internal	Internal use only	RW	
21	Internal	Internal use only	RW	
22	Internal	Internal use only	RW	
23	Internal	Internal use only	RW	

Note: There is no default value.

6.3.2. Register24~31: EEPROM VLAN (Bytes30~44) Register

Table 24. Register24~31: EEPROM VLAN (Bytes30~44) Register

Reg.bit	Name	Description	Mode	Default
24.15~24.12	Reserved		RO	1111b
24.11~24.0	VIDA[11:0]	**VLAN Identifier of VLAN A:** Reg24.11=VIDA[11], Reg24.0=VIDA[0]. There is no default value.	RW	
25.7~25.5	Reserved		RO	111b
25.4~25.0	MemberA[4:0]	**Member Set of VLAN A:** MemberA[4:0] determines the VLAN member of VLAN A. For example, MemberA[4:0]=10001 means port4 and port0 are members of VLAN A. MemberA[4:0]=10010 means port4 and port1 are members of VLAN A. MemberA[4:0]=11111 means all ports are members of VLAN A.	RW	10001b
26.7~26.4	Reserved		RO	1111b
26.3~26.0 25.15~25.8	VIDB[11:0]	**VLAN Identifier of VLAN B:** There is no default value.	RW	
26.15~26.13	Reserved		RO	111b
26.12~26.8	MemberB[4:0]	**Member Set of VLAN B:** MemberB[4:0]=10010 means port4 and port1 are members of VLAN B.	RW	10010b
27.15~27.12	Reserved		RO	1111b
27.11~27.0	VIDC[11:0]	**VLAN Identifier of VLAN C:** There is no default value.	RW	
28.7~28.5	Reserved		RO	111b
28.4~28.0	MemberC[4:0]	**Member Set of VLAN C:** MemberC[4:0]=10100 means port4 and port2 are members of VLAN C.	RW	10100b
29.7~29.4	Reserved		RO	1111b
29.3~29.0 28.15~28.8	VIDD[11:0]	**VLAN Identifier of VLAN D:** There is no default value.	RW	
29.15~29.13	Reserved		RO	111b
29.12~29.8	MemberD[4:0]	**Member Set of VLAN D:** MemberD[4:0]=11000 means port4 and port3 are members of VLAN D.	RW	11000b
30.15~30.12	Reserved		RO	1111b
30.11~30.0	VIDE[11:0]	**VLAN Identifier of VLAN E:** There is no default value.	RW	
31.15~31.5	Reserved		RO	11111111111b
31.4~31.0	MemberE[4:0]	**Member Set of VLAN E:** MemberE[4:0]=11111 means all ports are members of VLAN E.	RW	11111b

6.4. PHY2: Pin & EEPROM Register

6.4.1. Register16: Pin Register

The RTL8305SB will load the value from pins upon reset, but can be updated via SMI after reset. This register needs a soft reset.

Table 25. Register16: Pin Register

Reg.bit	Name	Description	Mode	Default
16.15	Internal	Internal use only	RW	1b
16.14	Internal	Internal use only	RW	1b
16.13	Internal	Internal use only	RW	1b
16.12	Internal	Internal use only	RW	1b
16.11	Reserved	Internal use only	RW	1b
16.10	Reserved		RO	1b
16.9 16.8	Qweight[1] Qweight[0]	**Weighted Round Robin Ratio of Priority Queue:** The frame service rate of High-pri queue: Low-pri queue 11: 16:1 10: Always high priority queue first 01: 8:1 00: 4:1 Pin Register.	RW	11b
16.7	DisFCAutoOff	**Disable Auto Turn Off Function of Flow Control Ability:** 1: Disable 0: Enable Enables Auto turn off of low priority queue's flow control ability for 1~2 sec whenever the port receives a high priority frame. The flow control ability is re-enabled when no high priority frame has been received for 1~2 sec. Pin Register.	RW	1b
16.6	DisDSPri	**Disable Differentiated Service Priority:** 1: Disable DS priority 0: Enable DS priority Pin Register.	RW	1b
16.5	DisTagPri	**Disable 802.1p VLAN Tag Priority Based QoS Function:** 1: Disable 0: Enable Pin Register.	RW	1b
16.4	DisPortPri[4]	**Disable Port-Based Priority QoS Function for Port4:** DisPortPri[4]: 1: Disable port4 priority 0: Enable port4 priority	RW	1b
16.3	DisPortPri[3]	**Disable Port-Based Priority QoS Function for Port3:** DisPortPri[3]: 1: Disable port3 priority 0: Enable port3 priority	RW	1b
16.2	DisPortPri[2]	**Disable Port-Based Priority QoS Function for Port2:** DisPortPri[2]: 1: Disable port2 priority 0: Enable port2 priority	RW	1b
16.1	DisPortPri[1]	**Disable Port-Based Priority QoS Function for Port1:** DisPortPri[1]: 1: Disable port1 priority 0: Enable port1 priority	RW	1b

Reg.bit	Name	Description	Mode	Default
16.0	DisPortPri[0]	**Disable Port-Based Priority QoS Function for Port0:** DisPortPri[0]: 1: Disable port0 priority 0: Enable port0 priority Pin Register.	RW	1b

6.4.2. Register17: Pin & EEPROM (Byte 45) Register for VLAN

Table 26. Register17: Pin & EEPROM (Byte 45) Register for VLAN

Reg.bit	Name	Description	Mode	Default
17.15~17.8	Reserved		RO	1111 1111b
17.7	DisSpecialTag	**Disable Special VLAN Tag Insert:** 1: Disable 0: Enable When this feature is enabled and set to **P4IRTag[1:0]=01**, egress packets coming from the LAN ports (ports with low priority) will not have a VLAN tag inserted. Un-tagged packets coming from the WAN ports (ports with high priority) will have special VLAN tags inserted (Ethernet Type=8101, PRI=0, CFI=0, and VID=0). Tagged packets coming from the WAN ports (ports with high priority) will have the Ethernet Type field of the VLAN tag (Ethernet Type=8102) modified.	RW	1b
17.6	Internal	Internal use only	RW	1b
17.5	DisVLAN	**Disable VLAN:** 1: Disable VLAN 0: Enable VLAN	RW	1b
17.4	DisTagAware	**Disable Tag Aware:** 1: Disable the 802.1Q tagged-VID Aware function. The RTL8305SB will not check the tagged VID of received frames to do VLAN classification. The RTL8305SB will always use Port-Based VLAN mapping. 0: Enable the Member Set Filtering function of the VLAN Ingress Rule. The RTL8305SB will check the tagged VID of received frames to do VLAN classification. The RTL8305SB will use tagged-VID VLAN mapping for tagged frames, and will use Port-Based VLAN mapping for untagged and priority-tagged frames.	RW	1b
17.3	DisMemFilter	**Disable Member Set Filtering:** 1: Disable the Member Set Filtering function of the VLAN Ingress Rule. The RTL8305SB will not discard any frames associated with a VLAN for which that port is not in the member set. 0: Enable the Member Set Filtering function of the VLAN Ingress Rule. The RTL8305SB will discard any frames associated with a VLAN for which that port is not in the member set.	RW	1b
17.2	DisTagAdmitCtrl	**Disable Tag Admit Control: Acceptable Frame Type:** 1: Disable Tag Admit Control: Acceptable Frame Type is “Admit All”. The RTL8305SB will receive all frames. 0: Enable Tag Admit Control: Acceptable Frame Type is “Admit All Tagged”. The RTL8305SB will receive only VLAN-tagged frames and drop all other untagged frames and priority tagged (VID=0) frames.	RW	1b

Reg.bit	Name	Description	Mode	Default
17.1	DisLeaky	**Disable Leaky VLAN:** 1: Disables forwarding of unicast frames to other VLANs. 0: Enables forwarding of unicast frames to other VLANs. Broadcast and multicast frames adhere to the VLAN configuration.	RW	1b
17.0	DisARP	**Disable ARP Broadcast to all VLAN:** 1: Disables broadcasting of ARP broadcast packets to all VLANs. 0: Enables broadcasting of ARP broadcast packets to all VLANs. ARP broadcast frame: DID=F.	RW	1b

6.5. PHY3: Port Control Register

6.5.1. Register16: Port Control Register

This register does not need a soft reset.

Table 27. Register16: Port Control Register

Reg.bit	Name	Description	Mode	Default
16.15	SoftReset	**Soft Reset:** 1: Soft reset. This bit is self-clearing.	RW/SC	0b
16.14~16.10	Reserved		RO	
16.9	DisP4LoopBack	**Disable Port4 Loopback:** 1: Disable port4 loopback function for normal application 0: Enable port4 loopback function for diagnostic application	RW	1b
16.8	DisP3LoopBack	**Disable Port3 Loopback:** 1: Disable port3 loopback function for normal application 0: Enable port3 loopback function for diagnostic application	RW	1b
16.7	DisP2LoopBack	**Disable Port2 Loopback:** 1: Disable port2 loopback function for normal application 0: Enable port2 loopback function for diagnostic application	RW	1b
16.6	DisP1LoopBack	**Disable Port1 Loopback:** 1: Disable port1 loopback function for normal application 0: Enable port1 loopback function for diagnostic application	RW	1b
16.5	DisP0LoopBack	**Disable Port0 Loopback:** 1: Disable port0 loopback function for normal application 0: Enable port0 loopback function for diagnostic application	RW	1b
16.4	EnPort4	**Enable Link of Port4:** 1: Enable Port4's PHY (UTP or FX) to provide the Link status to MAC for normal operation 0: Disable Port4's PHY (UTP or FX) to provide the Link status to MAC. This port status is link failed for MAC, but PHY still works normally The link status of MII MAC/MII PHY/SNI PHY is determined by the P4LNKSTA pin	RW	1b
16.3	EnPort3	**Enable Link of Port3:** 1: Enable Port3's PHY (UTP or FX) to provide the Link status to MAC for normal operation 0: Disable Port3's PHY (UTP or FX) to provide the Link status to MAC. This port is linked fail for MAC, but PHY still works normally	RW	1b

Reg.bit	Name	Description	Mode	Default
16.2	EnPort2	**Enable Link of Port2:** 1: Enable Port2's PHY (UTP or FX) to provide the Link status to MAC for normal operation 0: Disable Port2's PHY (UTP or FX) to provide the Link status to MAC. This port is linked fail for MAC, but PHY still works normally	RW	1b
16.1	EnPort1	**Enable Link of Port1:** 1: Enable Port1's PHY (UTP or FX) to provide the Link status to MAC for normal operation 0: Disable Port1's PHY (UTP or FX) to provide the Link status to MAC. This port is linked fail for MAC, but PHY still works normally	RW	1b
16.0	EnPort0	**Enable Link of Port0:** 1: Enable Port0's PHY (UTP or FX) to provide the Link status to MAC for normal operation 0: Disable Port0's PHY (UTP or FX) to provide the Link status to MAC. This port is linked fail for MAC, but PHY still works normally	RW	1b

6.5.2. Register17: EEPROM (Byte 46) Register

Table 28. Register17: EEPROM (Byte 46) Register

Reg.bit	Name	Description	Mode	Default
17.15~17.7	Reserved		RO	1111 1111 1b
17.6	Internal	Internal use only	RW	1b
17.5~17.3	Internal	Internal use only	RW	
17.2~17.0	Internal	Internal use only	RW	

6.5.3. Register18~20: EEPROM (Bytes47~52) Register

Table 29. Register18~20: EEPROM (Bytes47~52) Register

Reg.bit	Name	Description	Mode	Default
18	Internal	Internal use only	RW	
19	Internal	Internal use only	RW	
20	Internal	Internal use only	RW	

7. Functional Description

7.1. Switch Core Functional Overview

7.1.1. Application

The RTL8305SB Ver.D is a 5-port Fast Ethernet switch controller that integrates memory, five MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip. All ports support 100Base-FX, which shares pins (TX+-/RX+-) with UTP ports and needs no SD+/- pins, a development using Realtek proprietary technology. To compensate for the lack of auto-negotiation in 100Base-FX applications, the RTL8305SB Ver.D can be forced into 100Base-FX half or full duplex mode, and can enable or disable flow control in fiber mode.

The five ports are separated into 3 groups (GroupX/GroupY/Port4) for flexible port configuration using strapping pins upon reset. The SetGroup pin is used to select the ports for GroupX and GroupY:

SetGroup=1: GroupX=Port0; GroupY=Ports 1, 2, and 3.

SetGroup=0: GroupX=Ports 0 and 1; GroupY=Ports 2 and 3.

The GxMode/GyMode/P4Mode[1:0] pins are used to select the operation mode (UTP/FX for GroupX and GroupY, UTP/FX/PHY mode MII/PHY mode SNI/MAC mode MII for Port4). Upon reset, in addition to using strapping pins, the RTL8305SB Ver.D also can be configured with an EEPROM or read/write operation by a CPU through the MDC/MDIO interface.

For more detailed system application circuits, refer to System Application Diagrams, page 75.

Note: Upon reset: *defined as a short time after the end of a hardware reset.* ***After reset:*** *defined as the time after the "Upon Reset" time.*

7.1.2. Port4

Operation mode of port4: Each port has two parts: MAC and PHY. In UTP and FX mode, Port4 uses both the MAC and internal PHY parts like the other ports. In other modes, Port4 uses only the MAC part, which provides an external interface to connect to the external MAC or PHY. Two pins are used for these operation mode configurations: P4MODE[1:0].

Port4 supports an external MAC interface which can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with the external MAC of a routing engine, PHY of a HomePNA, or other physical layer transceiver.

If the MAC part of Port4 connects with an external MAC, such as the processor of a router application, it will act as a PHY. This is PHY mode MII, or PHY mode SNI. In PHY mode MII or PHY mode SNI, Port4 uses the MAC part only, and provides an external MAC interface to connect MACs of external devices. In order to connect both MACs, the MII of the switch MAC should be reversed into PHY mode.

If the MAC part of Port4 connects with an external PHY, such as the PHY of a HomePNA application, Port4 will act as a MAC. This is MAC mode MII. In MAC mode MII, Port4 uses its MAC to connect to an external PHY and ignores the internal PHY part.

External MAC interface: In order to act as a PHY when port4 is in PHY mode, some pins of the external MAC interface should be changed. For example, TXC are input pins for MAC but output pins for PHY. So the pin MTXC/PRXC is input for MAC mode and output for PHY mode. Refer to the following diagram to check the relationship between the RTL8305SB Ver.D and the external device.

Hint: Connect the input of the RTL8305SB Ver.D to the output of the external device. The RTL8305SB Ver.D has no RXER, TXER, and CRS pins for MII signaling. Because the RTL8305SB Ver.D does not support pin CRS, it is necessary to connect the MTXEN/PRXDV (output) of PHY mode to both CRS and RXDV (input) of the external device.

Port4 status pins: When P4MODE[1:0]=11, Port4 can be either UTP or MAC mode MII. Port4 will automatically detect the link status of UTP from the internal PHY and link status MAC mode MII from both the TXC of the external PHY and P4LNKSTA#. If both UTP and MII port are linked, UTP has higher priority and the RTL8305SB Ver.D will ignore the signal of the MII port.

In UTP and FX mode, the internal PHY will provide the port status (Link/Speed/Duplex/Full Flow Control ability) in real time. In order to provide the initial configuration of Port4's PHY (UTP or FX mode), four pins (P4ANEG, P4Full, P4Spd100, P4EnFC) are used to strap upon reset. However, three of these pins are also used for Port4's MAC (the other three modes) in real time after reset (P4Spd100 -> P4SpdSta, P4Full -> P4DupSta, P4EnFC -> P4FLCTRL).

In the other three modes, four pins (P4LNKSTA#, P4SpdSta, P4DupSta, P4FLCTRL) are necessary in order to provide the port status to Port4's MAC in real time. That means that the external MAC or PHY should be forced to the same port status as Port4's MAC.

Related pins: When port4 is in UTP or FX mode, the LEDs of port4 are used to display PHY status. When port4 is in other modes, the LEDs of port4 are used to display MAC status.

Four parallel LEDs corresponding to port4 can be three-stated (disable LED functions) for MII port application by setting ENP4LED in EEPROM to 0. In UTP applications, this bit should be 1.

Pin **SEL_MIIMAC#** can be used to indicate MII MAC port active after reset for the purposes of UTP/MII auto-detection.

One 25MHz clock output (pin CK25MOUT) can be used as a clock source for the underlying HomePNA/other PHY physical devices.

PHY mode MII/PHY mode SNI: In routing applications, the RTL8305SB Ver.D cooperates with a routing engine to communicate with the WAN (Wide Area Network) through MII/SNI. In such applications, P4LNKSTA# =0 and P4MODE[1] is pulled low upon reset. P4MODE[0] determines whether MII or SNI mode is selected.

In MII (nibble) mode (P4MODE[0]=1), P4SPDSTA=1 results in MII operating at 100Mbps with MTXC, and MRXC runs at 25MHz; however, P4SPDSTA=0 leads to MII operating at 10Mbps with MTXC, and MRXC runs at 2.5MHz.

In SNI (serial) mode (P4MODE[0]=0), P4SPDSTA has no effect and should be pulled-down. SNI mode operates at 10Mbps only, with MTXC and MRXC running at 10MHz. In SNI mode the RTL8305SB Ver.D does not loopback a RXDV signal as a response to TXEN, and does not support the heart-beat function (asserting COL signal for each complete TXEN signal).

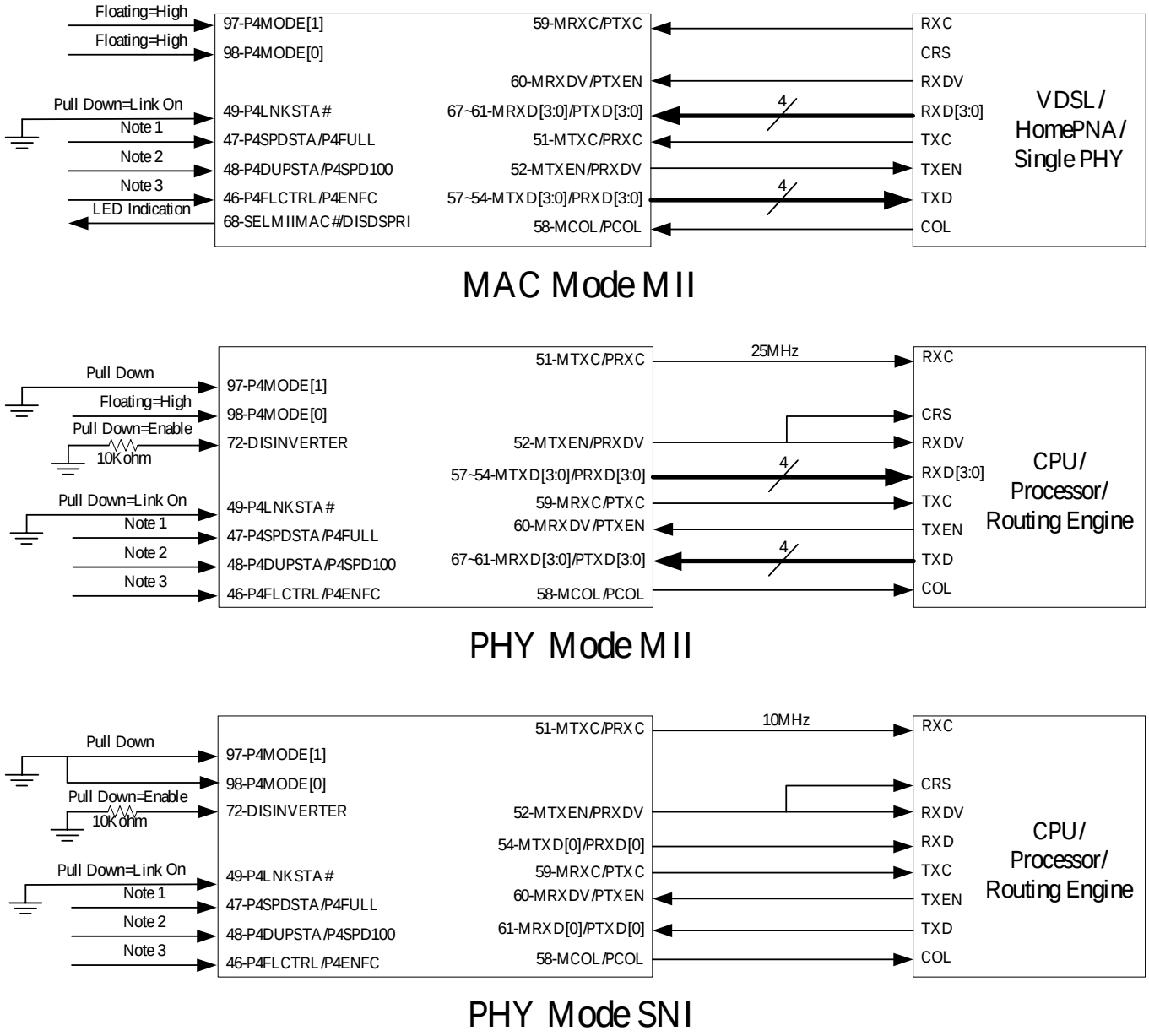


Figure 3. Port4 Operating Mode Overview

Note1: Pull high or floating to set speed to 100Mbps and pull low to set speed to 10Mbps.
Note2: Pull high or floating to set to full duplex and pull low to set to half duplex.
Note3: Pull high or floating to enable flow control in full duplex and pull low to disable.

MAC mode MII: In HomePNA or other PHY applications, the RTL8305SB Ver.D provides the MII interface to the underlying HomePNA or other physical device in order to communicate with other types of LAN media. In such applications, the P4MODE[1:0] pins are floating upon reset and the RTL8305SB Ver.D supports the UTP/MII auto-detection function. When both UTP and MII are active (link on), the UTP port has a higher priority than the MII port.

In HomePNA applications, P4SPDSTA must be pulled down as HomePNA is half-duplex only. P4DUPSTA should also be pulled down. P4LNKSTA# must be pulled down instead of being wired to the LINK LED pin of the HomePNA because of the unstable link state of HomePNA, a characteristic based on the HomePNA 1.0 standard. Because the HomePNA PHY physical layer is half duplex and can only detect a collision event during the AID header interval (the time when transmitting the Ethernet preamble), the back pressure flow control algorithm is not suitable for the HomePNA network and the P4FLCTRL pin should be pulled down.

For other PHY applications, P4SPDSTA, P4DUPSTA, and P4FLCTRL depend on the application.

7.1.3. Port Status Configuration

The RTL8305SB Ver.D supports flexible port status configuration for PHY by pin (GxANeg/GyANeg/P4ANeg, GxSpd100/GySpd100/P4Spd100, and GxFull/GyFull/P4Full) on a group basis upon reset, or by internal registers (Reg.0.12, Reg.0.13, Reg.0.8, and Reg.4.5/4.6/4.7/4.8) via SMI on a per port basis after reset. Those pins are used to assign the initial value of MII register0 and 4 (PHY registers) upon reset. The registers can be updated via SMI on a per port basis after reset. For example, the initial value of register0.12 of port4 will be 0 when pin P4Aneg is 1 upon reset.

All ports support 100Base-FX, which shares pins with UTP (TX+-/RX+-) and needs no SD+- pins (Realtek patent). 100Base-FX can be forced into half or full duplex mode with optional flow control ability. In order to operate correctly, both sides of the connection should be set to the same settings. In 100Base-FX, duplex and flow control ability can be set via strapped pins upon reset, or via SMI after reset. Note that 100Base-FX does not support Auto-Negotiation according to IEEE 802.3u. Pins GxANeg/GyANeg/P4Aneg as well as GxSpd100/GySpd100/P4Spd100 are not used for 100Base-FX mode and can be left floating while in 100Base-FX mode. For example: port4 will be forced into full duplex 100Base-FX with flow control ability when P4Mode[1:0]=10, P4Full=1, P4EnFC=1 upon reset (regardless of P4Spd100 and P4ANeg).

When Auto-Negotiation ability is enabled in UTP mode, the RTL8305SB Ver.D supports Auto-Negotiation and parallel detection of 10Base-T/100Base-TX to automatically determine line speed, duplex, and flow control. The parallel detection process is used when connecting a device that does not support auto-negotiation. For example: port0 is UTP with all abilities (default for normal switch applications: GxMode=1, GxANeg=1, GxSpd100=1, GxFull=1, GxEnFC=1. The content of MII registers will be Reg0.12=1, Reg4.5=1, Reg4.6=1, Reg4.7=1, Reg4.8=1, and Reg4.10=1). If the connecting device supports auto-negotiation, 10Full with 802.3x flow control ability, port0 will enter the auto-negotiation process. The result will be 10Full with 802.3x flow control ability for both devices. If the other device is 10M without auto-negotiation, port0 will enter the parallel detection process. The result will be 10Half without 802.3x flow control ability for port0.

Note: Each port can operate at 10Mbps or 100Mbps in full-duplex or half-duplex mode independently of others when auto-negotiation is on.

The port status for the PHY on a group basis can easily be set by pin configuration. For example, when group X is 100FX (GxMode=0), group X can be set as force mode half duplex by setting pin GxFull to 0. Group Y can also be set as UTP mode NWAY mode 10Full by setting GyMode=1, GyANeg=1, GySpd100=0, GyFull=1. Refer to the pin descriptions for details.

7.1.4. Enable Port

The RTL8305SB Ver.D supports internal registers for individual ports for MAC to mask the current Link status from the PHY. For example: If register EnPort0=0, the MAC of port0 will ignore Link status from the PHY and treat this port as no-link.

7.1.5. Flow Control

The RTL8305SB Ver.D supports IEEE 802.3x full duplex flow control, Force mode Full duplex Flow Control, and optional half duplex back pressure.

IEEE 802.3x Full Duplex Flow Control: For UTP with auto-negotiation ability (GxANeg/GyANeg/P4Aneg set to 1), the pause ability (Reg.4.10) of full duplex flow control is enabled by pins GxEnFC/GyEnFC/P4EnFC on a group basis upon reset, or internal registers via SMI on a per port basis after reset. For UTP with auto-negotiation ability, IEEE 802.3x flow control's ability is auto-negotiated between the remote device and the RTL8305SB Ver.D. If the auto-negotiation result of the 802.3x pause ability is "enabled" (Reg.4.10=1 and Reg.5.10=1), the full duplex 802.3x flow control function is enabled. Otherwise, the full duplex 802.3x flow control function is disabled.

Force Mode Full Duplex Flow Control: For UTP without auto-negotiation ability (GxANeg/GyANeg/P4Aneg is 0) and 100Base-FX, IEEE 802.3x flow control's ability can be forced to "enabled" on the RTL8305SB Ver.D by pins GxEnFC/GyEnFC/P4EnFC on a group basis upon reset, or internal registers (Reg.5.10) via SMI on a per port basis after reset. For example, port4 will be forced to 10Full UTP with forced mode full duplex flow control ability, regardless of the connected device, when P4Mode[1:0]=10, P4Aneg=0, P4Spd100=0, P4Full=1, P4EnFC=1. Port0 will be forced to 100Full FX with forced mode full duplex flow control ability, regardless of the connected device, when SetGroup=1, GxMode=0, GxFull=1, GxEnFC=1.

Regardless of IEEE 802.3x full duplex flow control or Force mode Full duplex Flow Control, when full duplex flow control is enabled, the RTL8305SB Ver.D will only recognize the 802.3x flow control PAUSE ON/OFF frames with DA=0180C2000001, type=8808, OP-code=01, PAUSE Time = maximum to zero, and with a good CRC.

If a PAUSE frame is received from any PAUSE flow control enabled port set to DA=0180C2000001, the corresponding port of the RTL8305SB Ver.D will stop its packet transmission until the PAUSE timer times out, or another PAUSE frame with zero PAUSE time is received. The RTL8305SB Ver.D will not forward any 802.3x PAUSE frames received from any port.

Half Duplex Back Pressure: If pin EnDefer is 1, the RTL8305SB Ver.D will send a preamble to defer the other station's transmission when there is no packet to send. Otherwise, if pin EnDefer is 0, the RTL8305SB Ver.D will force a collision with the other station's transmission when the buffer is full.

If pin 48pass1 is 0, the RTL8305SB Ver.D will always collide with JAM (Continuous collision). Otherwise, if pin 48pass1 is 1, the RTL8305SB Ver.D will try to forward one packet successfully after 48 forced collisions (48pass1), to avoid the connected repeater being partitioned due to excessive collisions.

NWAY Mode: For UTP with auto-negotiation ability, pins GxEnFC/GyEnFC/P4EnFC are effective only in Full duplex mode. Therefore, for UTP in half duplex mode, half duplex back pressure flow control is controlled by the ENBKPRS pin strap upon hardware reset.

Force Mode: For UTP without auto-negotiation ability, or in 100Base-FX mode, the operation mode can be forced to half duplex. Half duplex back pressure flow control can be forced to enabled on the RTL8305SB Ver.D side by pin GxEnFC/GyEnFC/P4EnFC on a group basis upon reset.

7.1.6. Address Search, Learning, and Aging

When a packet is received, the RTL8305SB Ver.D will use the least 10 bits of the destination MAC address to index the 1024-entry look-up table, and at the same time will compare the destination MAC address with the contents of the 16-entry CAM. If the indexed entry is valid or the CAM comparison is matched, the received packet will be forwarded to the corresponding destination port. Otherwise, the RTL8305SB Ver.D will broadcast the packet. This is the "Address Search".

The RTL8305SB Ver.D then extracts the least 10 bits of the source MAC address to index the 1024-entry look-up table. If the entry is not already in the table it will record the source MAC address and add switching information. If this is an occupied entry, it will update the entry with new information. This is called "Learning". If the indexed location has been occupied by a different MAC address (hash collision), the new source MAC address will be recorded into the 16-entry CAM. The 16-entry CAM reduces address hash collisions and improves switching performance.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if it's time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8305SB Ver.D is between 200 and 300 seconds.

7.1.7. Address Direct Mapping Mode

The RTL8305SB Ver.D uses the least 10 bits of the MAC address to index the 1024-entry look-up table. For example: the index of MAC address "12 34 56 78 90 ab" will be 0ab.

7.1.8. Half Duplex Operation

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called "truncated binary exponential backoff". At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slotTime (512 bit times). The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leqq r < 2^k$

where

k =min (n, backoffLimit). The 802.3 defines the backoffLimit as 10.

7.1.9. Inter-Frame Gap

The Inter-Frame Gap is 9.6μs for 10Mbps Ethernet and 960ns for 100Mbps Fast Ethernet.

7.1.10. Illegal Frame

Illegal frames such as CRC error packets, runt packets (length < 64 bytes) and oversize packets (length > maximum length) will be discarded.

7.1.11. Dual MII Interface

Home Gateways, broadband access routers, and SOHO routers generally contain a powerful Network Processor, with many I/O interfaces, including MII and SNI interfaces. Traditionally, this system connects one of the MII interfaces to a single PHY as the WAN port, and another interface connects to a multi-port switch as the LAN ports. In order to meet application demands, Realtek offers an advanced version of the RTL8305SB, the RTL8305SB Ver. D. The RTL8305SB Ver.D features Dual MII Interfaces to eliminate the need for a single PHY.

Figure 4 shows the traditional design of a SOHO router. In this case, the router needs an extra single PHY as the WAN port. A traditional 5-port switch has five MAC and five PHY circuits on a single chip. When port4 is configured as MII-MAC/MII-PHY/SNI-PHY, we only use the MAC part of port4.

The RTL8305SB Ver.D has pin 42, DISDUALMII, to support both port4 PHY and MAC circuits. When the Dual MII feature is enabled, the port4 PHY may be used as the WAN interface as shown in Figure 5.

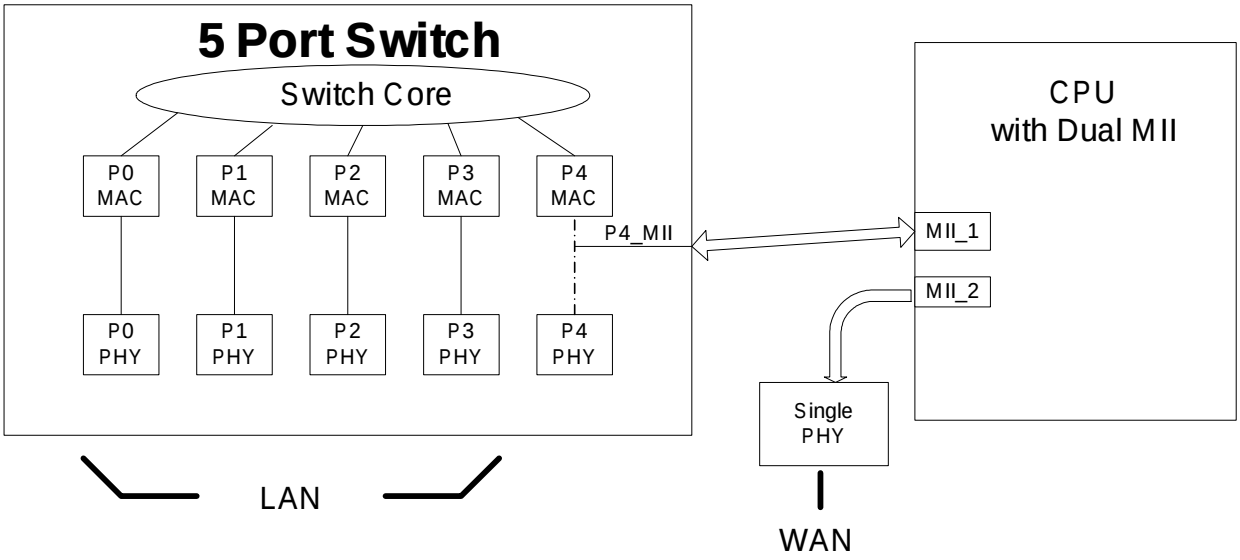


Figure 4. Traditional Application

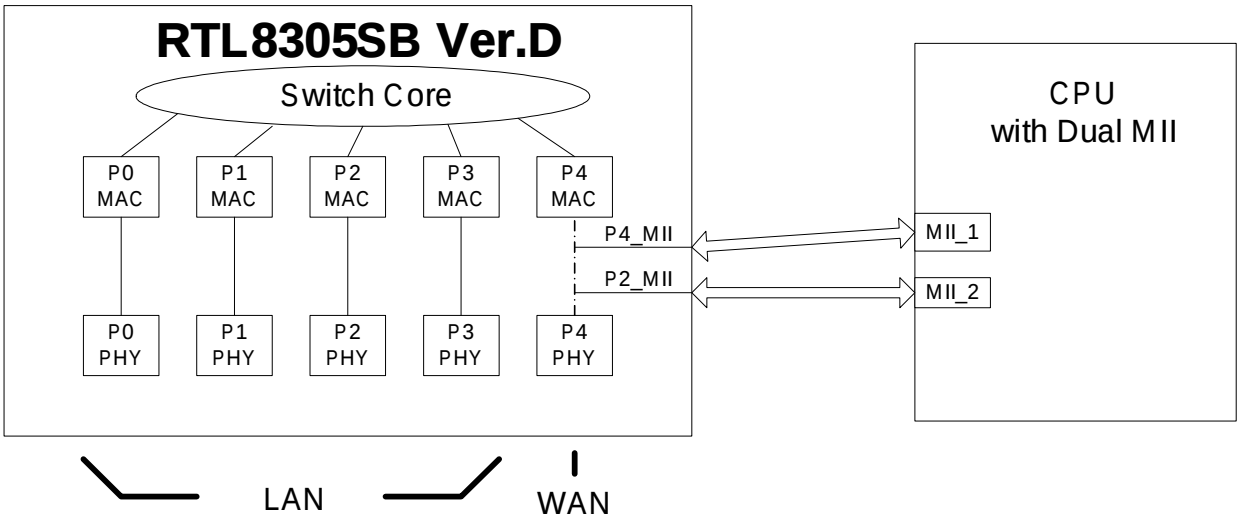


Figure 5. Dual MII Application Diagram

Dual MII Interfaces Configuration: Port4 of the RTL8305SB Ver.D is able to separate the MAC and PHY circuits via the DISDUALMII configuration. When DISDUALMII is configured as 0, the port4 MAC circuit supports MAC mode MII, PHY mode MII, or PHY mode SNI interface. The port4 PHY circuit supports an MII on the MAC side, and a UTP or fiber interface in the PHY transceiver. The following figures show the four types of configuration for the RTL8305SB Ver.D with a CPU application.

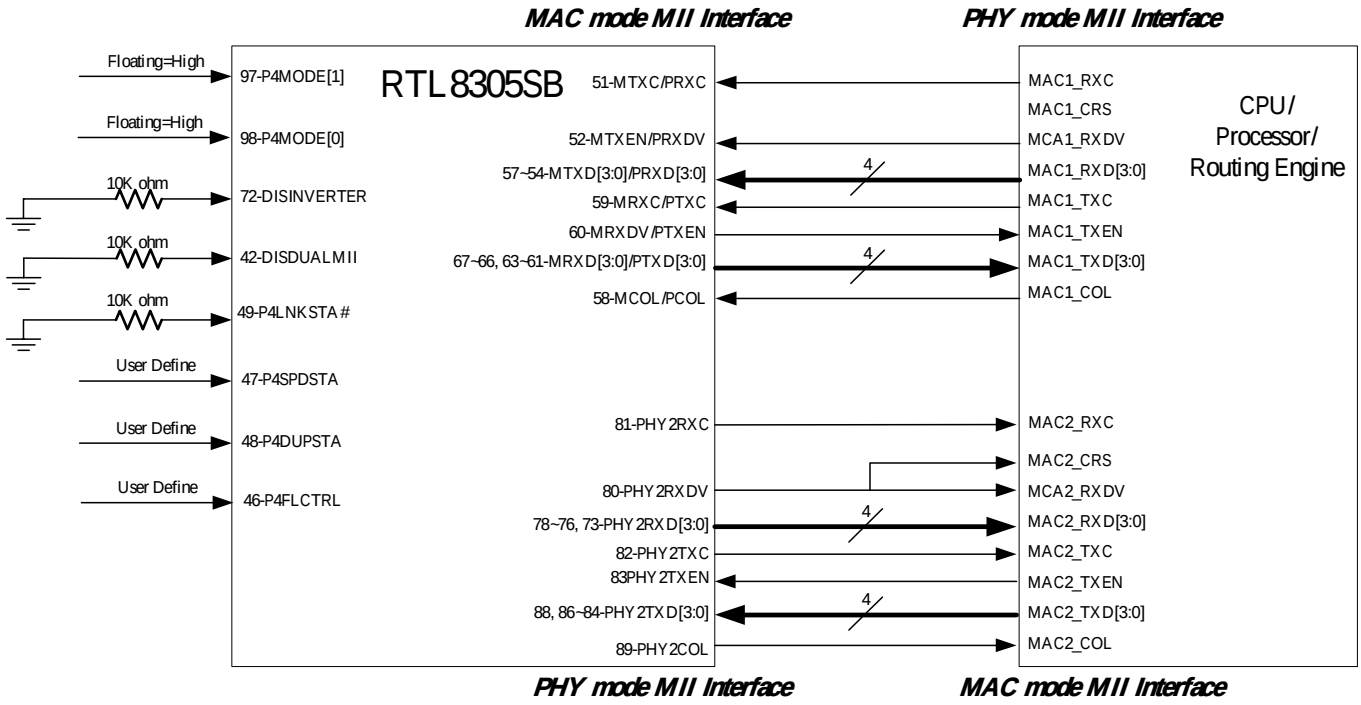


Figure 6. Dual MII Mode with 1 MII-MAC + 1 MII-PHY (100Base-T UTP) Interfaces Application Circuit

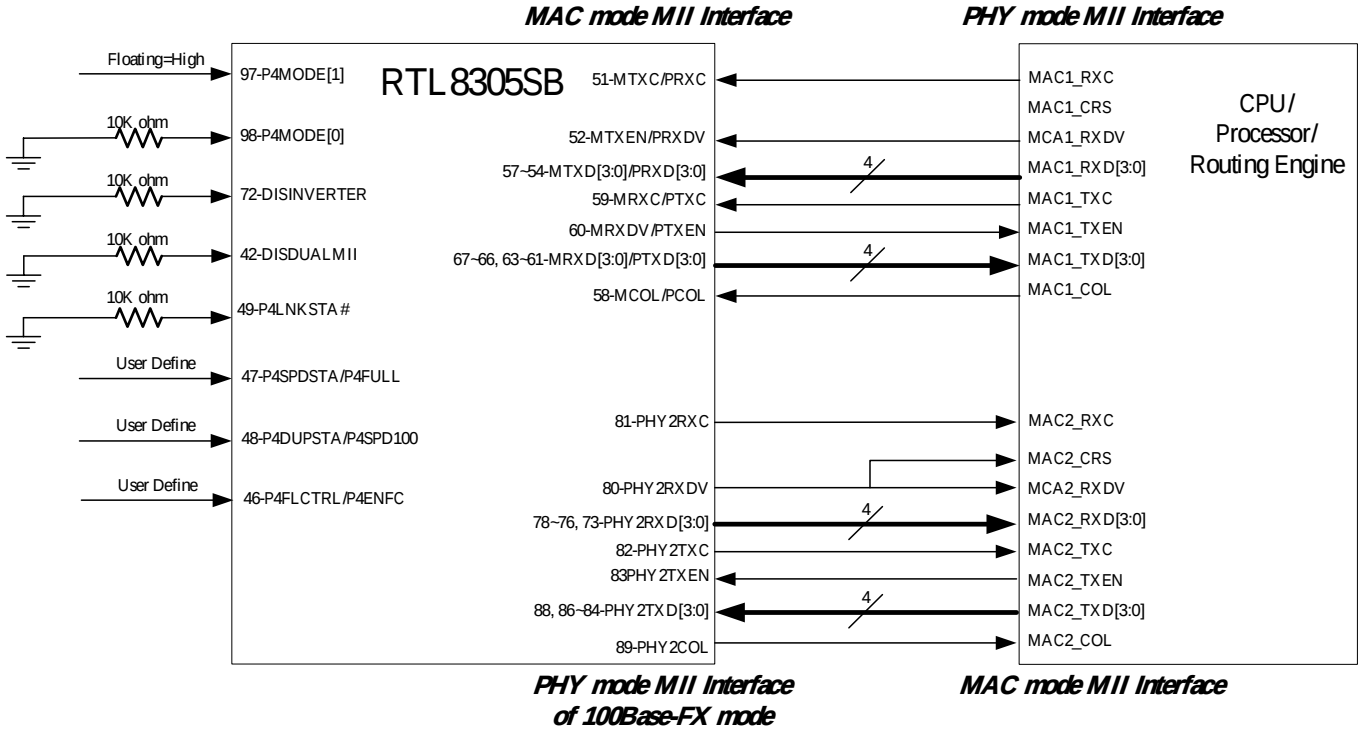


Figure 7. Dual MII Mode with 1 MII-MAC + 1 MII-PHY (100Base-FX mode) Interfaces Application Circuit

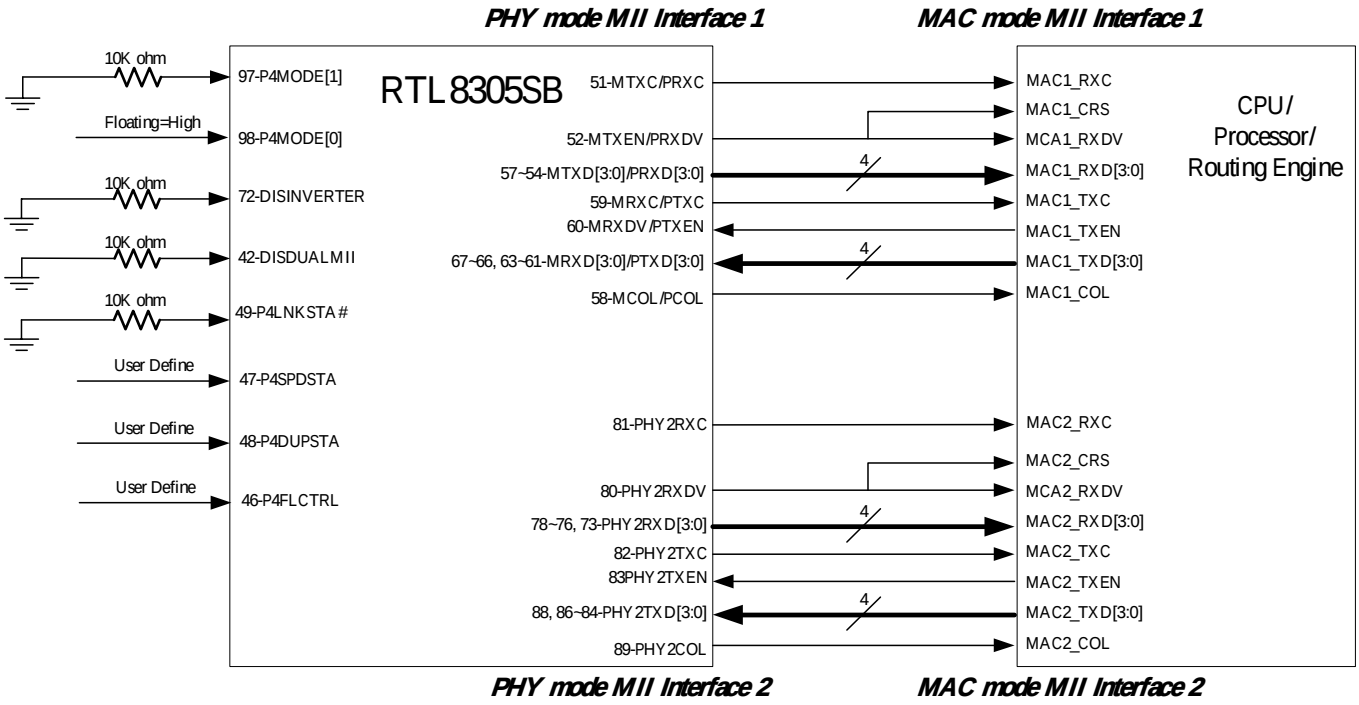


Figure 8. Dual MII Mode with 1 MII-PHY + 1 MII-PHY (100Base-T UTP) Interfaces Application Circuit

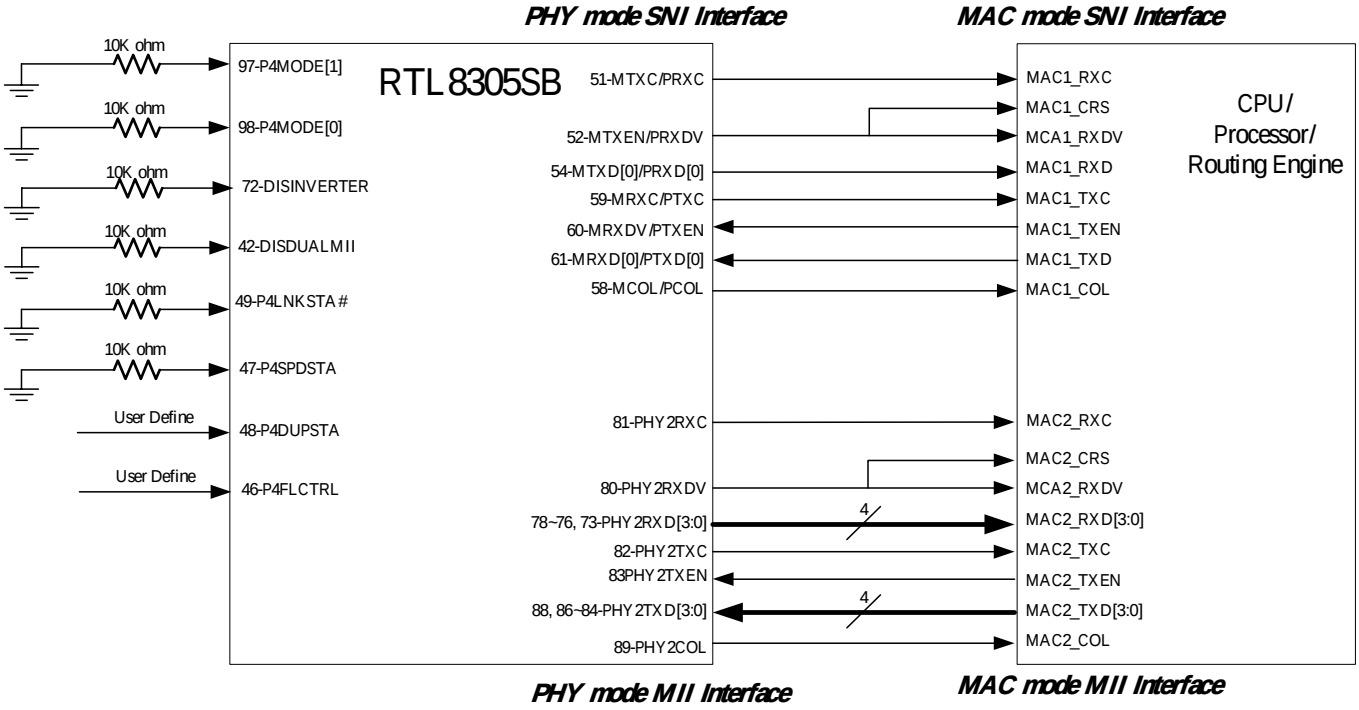


Figure 9. Dual MII Mode with 1 SNI-PHY + 1 MII-PHY (100Base-T UTP) Interfaces Application Circuit

Dual MII Registers Definition: For RTL8305SB Ver.D single MII interface applications (DISDUALMII=1), PHY4 MII registers represent the port4 MAC part (only link status, speed, duplex; i.e. Reg.1.2, Reg.0.13, Reg.0.8).

For RTL8305SB Ver.D dual MII interface applications (DISDUALMII=0), PHY 4 registers represent the port4 PHY part (***Read/Write***), and PHY5 registers represent the port4 MAC part (Reg.0, 1, 4, 5, ***Read Only***). The 100Base-FX mode of the PHY circuit (P4MODE[1:0]=10) only supports 100Mbps and full duplex. The PHY circuit of UTP mode only supports full ability NWay (Flow control enabled, both 10/100Mbps, both Full/Half duplex). Table 30 shows the MII PHY registers of PHY4 and PHY5 definitions when P4MODE[1:0] and DISDUALMII are configured in various combinations.

Table 30. MII Register Definition for PHY4 and PHY5

<table>
<tr><th>P4MODE[1:0]</th><th>DISDUALMII</th><th>PHY4 (Reg.0, 1, 4, 5)</th><th>PHY5 (Reg.0, 1, 4, 5)</th></tr>
<tr><td>11</td><td>1</td><td>P4LNKSTA#=1,
MII Registers for PHY circuit.
Fully support Reg.0, 1, 4, 5, for PHY.

P4LNKSTA#=0 and UTP link off,
MII Registers for MAC circuit.
Reg.0.13=P4SPDSTA,
Reg.0.8=P4DUPSTA,
Reg.1.2=P4LNKSTA#.</td><td>N/A</td></tr>
<tr><td>10</td><td>1</td><td>MII Registers for MAC circuit.
Reg.0.13=1,
Reg.0.8=P4DUPSTA,
Reg.1.2=Signal detection from fiber link.</td><td>N/A</td></tr>
<tr><td>01</td><td>1</td><td>MII Registers for MAC circuit.
Reg.0.13=P4SPDSTA,
Reg.0.8=P4DUPSTA,
Reg.1.2=P4LNKSTA#.</td><td>N/A</td></tr>
<tr><td>00</td><td>1</td><td>MII Registers for MAC circuit.
Reg.0.13=P4SPDSTA,
Reg.0.8=P4DUPSTA,
Reg.1.2=P4LNKSTA#.</td><td>N/A</td></tr>
<tr><td>11</td><td>0</td><td>MII Registers for PHY circuit in UTP mode.
Fully supports Reg.0, 1, 4, 5, for PHY.</td><td>MII Registers for MAC circuit.
Reg.0.13=P4SPDSTA,
Reg.0.8=P4DUPSTA,
Reg.1.2=P4LNKSTA#,
Reg.4.10 and 5.10=P4FLCTRL,
Reg.4.8~4.5 and Reg.5.8~5.5=
<table><tr><th>Reg.4.8~4.5
Reg.5.8~5.5</th><th>P4SPDSTA</th><th>P4DUPSTA</th></tr><tr><td>1111</td><td>1</td><td>1</td></tr><tr><td>0111</td><td>1</td><td>0</td></tr><tr><td>0011</td><td>0</td><td>1</td></tr><tr><td>0001</td><td>0</td><td>0</td></tr></table></td></tr>
<tr><td>10</td><td>0</td><td>MII Registers for PHY circuit in 100Base-FX mode.
Reg.0.13=1 (SPD=100Mbps),
Reg.0.8=1, (DUP=Full Duplex),
Reg.1.2=Signal detection from Fiber link.
Reg.4.10 and 5.10=P4FLCTRL.</td><td>MII Registers for MAC circuit.
Reg.0.13=P4SPDSTA,
Reg.0.8=P4DUPSTA,
Reg.1.2=P4LNKSTA#,
Reg.4.10 and 5.10=P4FLCTRL,
Reg.4.8~4.5 and Reg.5.8~5.5=
<table><tr><th>Reg.4.8~4.5
Reg.5.8~5.5</th><th>P4SPDSTA</th><th>P4DUPSTA</th></tr><tr><td>1111</td><td>1</td><td>1</td></tr><tr><td>0111</td><td>1</td><td>0</td></tr><tr><td>0011</td><td>0</td><td>1</td></tr><tr><td>0001</td><td>0</td><td>0</td></tr></table></td></tr>
</table>

<table>
<tr><th>P4MODE[1:0]</th><th>DISDUALMII</th><th>PHY4 (Reg.0, 1, 4, 5)</th><th>PHY5 (Reg.0, 1, 4, 5)</th></tr>
<tr><td>01</td><td>0</td><td>MII Registers for PHY circuit in UTP mode.
Fully supports Reg.0, 1, 4, 5, for PHY</td><td>Reg.0.13=P4SPDSTA,
Reg.0.8=P4DUPSTA,
Reg.1.2=P4LNKSTA#,
Reg.4.10 and 5.10=P4FLCTRL,
Reg.4.8~4.5 and Reg.5.8~5.5=
<table>
<tr><th>Reg.4.8~4.5
Reg.5.8~5.5</th><th>P4SPDSTA</th><th>P4DUPSTA</th></tr>
<tr><td>1111</td><td>1</td><td>1</td></tr>
<tr><td>0111</td><td>1</td><td>0</td></tr>
<tr><td>0011</td><td>0</td><td>1</td></tr>
<tr><td>0001</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>00</td><td>0</td><td>MII Registers for PHY circuit in UTP mode.
Fully supports Reg.0, 1, 4, 5, for PHY</td><td>Reg.0.13=P4SPDSTA,
Reg.0.8=P4DUPSTA,
Reg.1.2=P4LNKSTA#,
Reg.4.10 and 5.10=P4FLCTRL,
Reg.4.8~4.5 and Reg.5.8~5.5=
<table>
<tr><th>Reg.4.8~4.5
Reg.5.8~5.5</th><th>P4SPDSTA</th><th>P4DUPSTA</th></tr>
<tr><td>1111</td><td>1</td><td>1</td></tr>
<tr><td>0111</td><td>1</td><td>0</td></tr>
<tr><td>0011</td><td>0</td><td>1</td></tr>
<tr><td>0001</td><td>0</td><td>0</td></tr>
</table></td></tr>
</table>

7.2. Physical Layer Functional Overview

7.2.1. Auto-Negotiation for UTP

The RTL8305SB Ver.D obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3u specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8305SB Ver.D advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability.

7.2.2. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven into the network media. The internal filter shapes the driven signals to reduce EMI emission, eliminating the need for an external filter.

7.2.3. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.2.4. Link Monitor

The 10Base-T link pulse detection circuit continually monitors the RXIP/RXIN pins for the presence of valid link pulses. Auto-polarity is implemented to correct the detected reverse polarity of RXIP/RXIN signal pairs.

7.2.5. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also benefits EMI emission.

7.2.6. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A De-scrambler, 5B/4B decoder and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.2.7. 100Base-FX

All ports support 100Base-FX, which shares pins with UTP (TX+-/RX+-) and needs no SD+- pins. 100Base-FX can be forced to half or full duplex with optional flow control ability.

Note: In compliance with IEEE 802.3u, 100Base-FX does not support Auto-Negotiation. In order to operate correctly, both sides of the connection should be set to the same duplex and flow control ability.

A scrambler is not needed in 100Base-FX. Compared to common 100Base-FX applications, the RTL8305SB Ver.D removes a pair of differential SD (Signal Detect) signals that provide a link monitoring function, which reduces the pin count (Realtek patent).

7.2.8. 100Base-FX Transmit Function

In 100Base-FX transmissions, dibits of TXD are processed as 100Base-TX except without being scrambled before the NRZI stage. Instead of converting to MLT-3 signals as in 100Base-TX, the serial data stream is driven out as NRZI PECL signals, which enter the fiber transceiver in differential-pairs form. The fiber transceiver may be 3.3V or 5V capable. Refer to 100Base-FX Application, on page 73 for example applications.

Table 31. PECL DC Characteristics

Parameter	Symbol	Min	Max	Unit
PECL Input High Voltage	Vih	Vdd-1.16	Vdd-0.88	V
PECL Input Low Voltage	Vil	Vdd-1.81	Vdd-1.47	V
PECL Output High Voltage	Voh	Vdd-1.02		V
PECL Output Low Voltage	Vol		Vdd-1.62	V

7.2.9. 100Base-FX Receive Function

Signals are received through PECL receiver inputs from a fiber transceiver and directly passed to a clock recovery circuit for data/clock recovery. Scrambling/de-scrambling is bypassed in 100Base-FX.

7.2.10. 100Base-FX Far-End-Fault-Indication (FEFI)

MII Reg.1.4 (Remote Fault) is the FEFI bit for ports when 100FX is enabled, and indicates that a FEFI has been detected. FEFI is an alternative in-band signaling that is composed of 84 consecutive 1's followed by one '0'. When the RTL8305SB Ver.D has detected this pattern three times, Reg.1.4 is set, which means the transmit path (Remote side's receive path) has problems. On the other hand, to send an FEFI stream pattern, the following condition needs to be satisfied; the incoming signal fails to cause Link OK, which in turn causes the remote side to detect a Far-End-Fault. This means that the receive path has a problem from the view of the RTL8305SB Ver.D. The FEFI mechanism is used only in 100Base-FX.

7.2.11. Reduced Fiber Interface

The RTL8305SB Ver.D ignores the underlying SD signal of the fiber transceiver to complete link detection and connection. This is achieved by monitoring RD signals from the fiber transceiver and checking whether any link integrity events are found. This significantly reduces pin-count, especially for high-port PHY devices. This is a Realtek patent-pending technology and available only with Realtek product solutions.

7.2.12. Power-Saving Mode

The RTL8305SB Ver.D implements power saving mode on a per port basis. A port automatically enters power saving mode 10 seconds after the cable is disconnected from it. Once a port enters power saving mode, it transmits normal link pulses only on its TXOP/TXON pins and continues to monitor the RXIP/RXIN pins to detect incoming signals, which might be the 100Base-TX MLT-3 idle pattern, 10Base-T link pulses, or Auto-Negotiation's FLP (Fast Link Pulse). After it detects an incoming signal, it wakes up from power saving mode and operates in normal mode according to the result of the connection.

7.2.13. Reg.0.11 Power-Down Mode

The RTL8305SB Ver.D implements power-down mode on a per port basis. Setting MII Reg.0.11 forces the corresponding port of the RTL8305SB Ver.D to enter power-down mode. This disables all transmit/receive functions, except SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface).

7.2.14. Crossover Detection and Auto Correction

During the link setup phase, the RTL8305SB Ver.D checks whether it receives active signals on every port in order to determine if a connection can be established. In cases where the receiver data pin pair is connected to the transmitter data pin pair of the peer device and vice versa, the RTL8305SB Ver.D will automatically change its configuration to swap receiver data pins with transmitter data pins. In other words, the RTL8305SB Ver.D adapts automatically to a peer device's configuration. If a port is connected to a PC or NIC with MDI-X interface with a crossover cable, the RTL8305SB Ver.D will reconfigure the port to ensure proper connection. This will effectively replace the DIP switch commonly used for reconfiguring a port on a hub or switch.

By pulling-up EN_AUTOXOVER, the RTL8305SB Ver.D identifies the type of connected cable and sets the port to MDI or MDIX. When switching to MDI mode, the RTL8305SB Ver.D uses TXOP/N as transmit pairs; when switching to MDIX mode, the RTL8305SB Ver.D uses RXIP/N as transmit pairs. This function is port-based. Pulling-down EN_AUTOXOVER disables this function and the RTL8305SB Ver.D operates in MDI mode, in which TXOP/N represents transmit pairs and RXIP/N represents receive pairs.

IEEE 802.3 compliant forced mode 100M ports with Autoxover have link issues with NWAY (Auto-Negotiation) ports. It is recommended to *not* use Autoxover for forced 100M.

7.2.15. Polarity Detection and Correction

For better noise immunity and lower interference to ambient devices, the Ethernet electrical signal on a twisted pair cable is transmitted in differential forms. That is, the signal is transmitted on two wires in each direction with inverse polarities (+/-). If wiring on the connector is faulty or a faulty transformer is used, the two inputs to a transceiver may carry signals with opposite but incorrect polarities. As a direct consequence, the transceiver will not work properly.

When the RTL8305SB Ver.D operates in 10Base-T mode, it automatically reverses the polarity of its two receiver input pins if it detects that the polarities of the incoming signals on the pins is incorrect. However, this feature is unnecessary when the RTL8305SB Ver.D is operating in 100Base-TX mode.

7.3. Advanced Functional Overview

7.3.1. Reset

The whole or just part of the RTL8305SB Ver.D is initialized depending on the reset type. There are several ways to reset the RTL8305SB Ver.D: hardware reset for the whole chip by pin RESET#, soft reset for all except PHY by register SoftReset, and PHY software reset for each PHY by register reset.

Hardware Reset: Pin RESET# = 0 set to RESET# = 1 (for at least 1ms). The RTL8305SB Ver.D resets the whole chip and then gets initial values from pins and serial EEPROM.

Soft Reset: Write bit15 of Reg16 of PHY3 as 1. The RTL8305SB Ver.D resets all except PHY and does not load EEPROM and Pin Registers with serial EEPROM and Pins. The SoftReset, EEPROM, and Pin registers are designed to provide a convenient way for users who want to use SMI to change the configuration. After changing the EEPROM or Pin registers via SMI (Serial Management Interface), the external device has to perform a soft reset in order to update the configuration.

PHY Software Reset: Write bit15 of Reg0 of a PHY as 1. The RTL8305SB Ver.D will then reset this PHY.

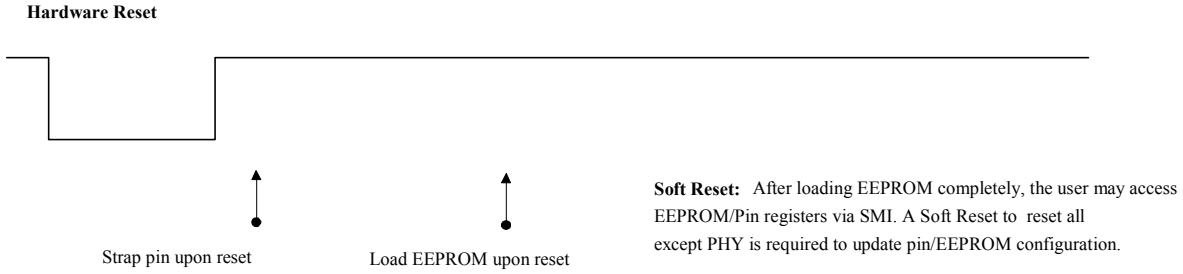


Figure 10. Reset

Some setting values for operation modes are latched from those corresponding mode pins upon hardware reset. Upon reset is defined as a short time after the end of a hardware reset. Other advanced configuration parameters may be latched from serial EEPROM if pin EnEEPROM=1.

7.3.2. Setup and Configuration

The RTL8305SB Ver.D can be configured easily and flexibly by hardware pins upon reset, optional serial EEPROM upon reset, and internal registers (including PHY registers for each port and MAC register for global) via SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface). There are three ways to configure:

- Only hardware pins for normal switch applications
- Hardware pins and serial EEPROM for advanced switch applications
- Hardware pins and internal registers via SMI for applications with processor

Four types of pins, each with internal pull-high resistors, are used for configuration:

1. Input pins used for strapping only upon reset (unused after reset)
2. Input pins (P4DUPSTA/P4FULL, P4SPDSTA/P4SPD100, P4FLCTRL/P4EnFC) used for strapping upon reset and used as input pins after reset. For example, pin P4DUPSTA/P4FULL is used as P4FULL upon reset for PHY of Port4 UTP/FX mode and used as P4DUPSTA for MAC of other mode after reset
3. Input/Output pins (MTXD[3:2]/PRXD[3:2]/P4IRTag[1:0], MTXD[1:0]/PRXD[1:0]/LEDMode[1:0]) used for strapping upon reset and used as output pins after reset
4. Input/Output pins (all LEDs) used for strapping upon reset and used as LED indicator pins after reset. The LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status

Pins with default value=1 are internal pull-high and use I/O pads. They can be left floating to set input value as high, but should not be connected to GND without a pull-down resistor.

The serial EEPROM shares two pins, SCL_MDC and SDA_MDIO, with SMI, and is optional for advanced configuration. SCL_MDC and SDA_MDIO are tri-state during hardware reset (pin RESET#=0). The RTL8305SB Ver.D will try to automatically find the serial EEPROM upon reset only if pin EnEEPROM=1. If the NoEEPROM bit of the serial EEPROM (bit 0 of the first byte) is 0, the RTL8305SB Ver.D will load all contents of the serial EEPROM into internal registers. Otherwise, the RTL8305SB Ver.D will use the default internal values.

Internal registers can still be accessed after reset via SMI (pin SCL_MDC and SDA_MDIO). Serial EEPROM signals and SMI signals must not exist at the same time. In order to use the SMI to flexibly change configuration, internal registers include the contents of some pins and all serial EEPROM. These registers do not work in real time and a Soft Reset is necessary after changing the EEPROM or Pin registers.

7.3.3. Example of Serial EEPROM: 24LC02

The 24LC02 interface is a 2-wire serial EEPROM interface providing 2K bits of storage space. The 24LC02 must be 2.5V compatible.

7.3.4. 24LC02 Device Operation

Clock and Data transitions: The SDA pin is normally pulled high with an external resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start condition: A high-to-low transition of SDA with SCL high is the start condition and must precede any other command.

Stop condition: A low-to-high transition of SDA with SCL high is a stop condition.

Acknowledge: All addresses and data are transmitted serially to and from the EEPROM in 8-bit words. The 24LC02 sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Random Read: A random read requires a "dummy" byte write sequence to load in the data word address.

Sequential Read: For the RTL8305SB Ver.D, the sequential reads are initiated by a random address read. After the 24LC02 receives a data word, it responds with an acknowledgement. As long as the 24LC02 receives an acknowledgement, it will continue to increment the data word address and clock out sequential data words in series.

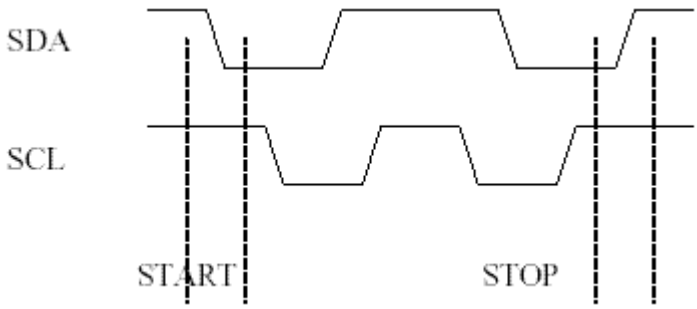


Figure 11. Start and Stop Definition

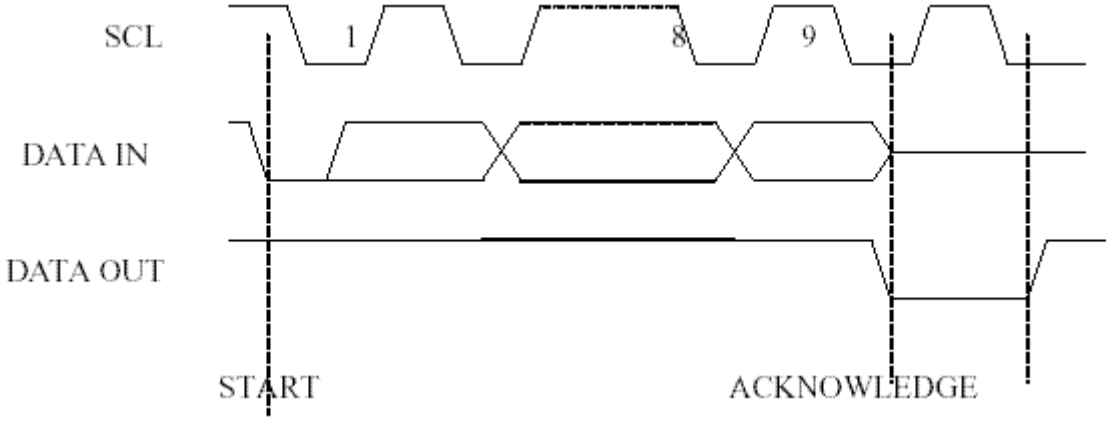


Figure 12. Output Acknowledge

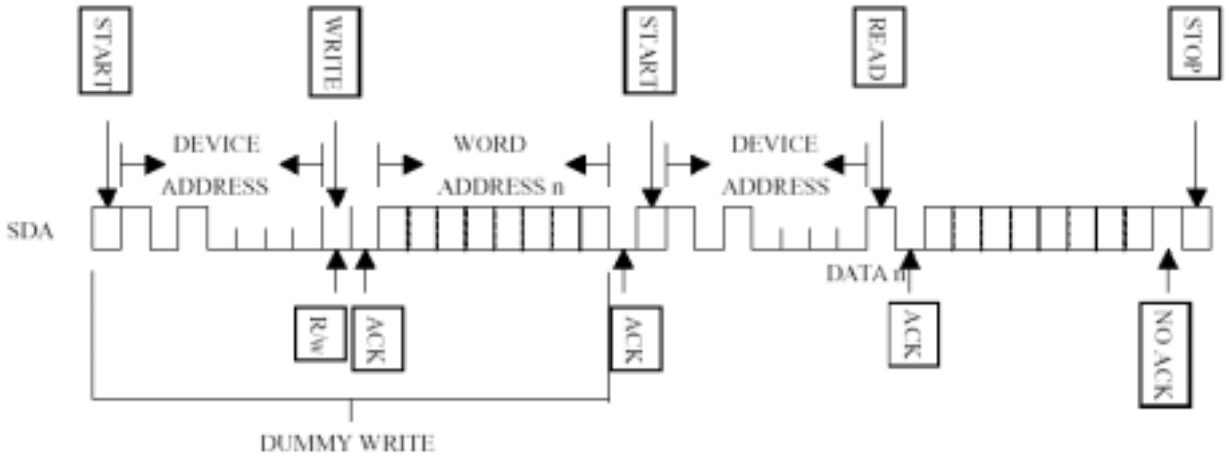


Figure 13. Random Read

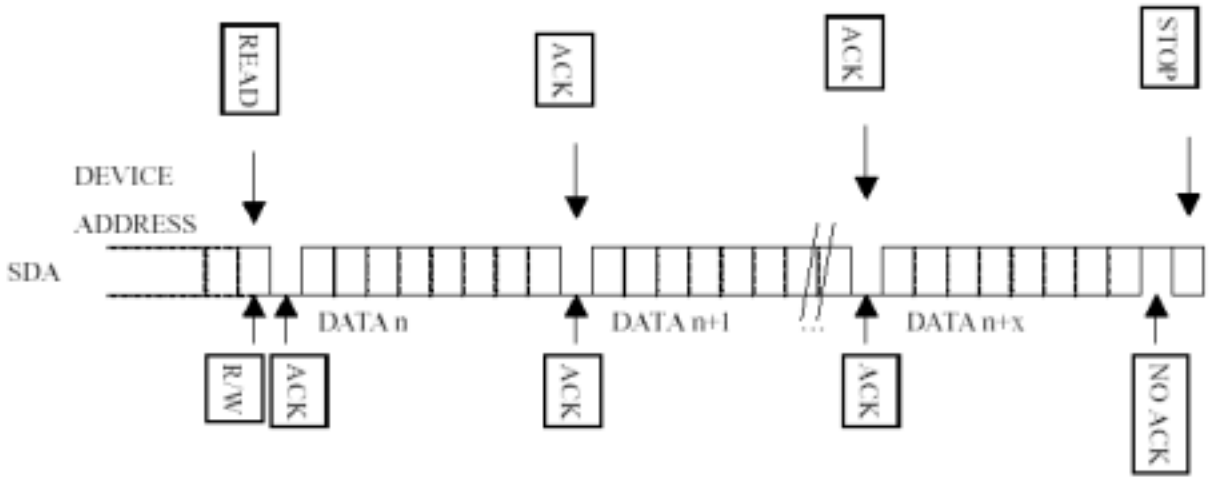


Figure 14. Sequential Read

7.3.5. SMI

The SMI (Serial Management Interface) is also known as the MII Management Interface, and consists of two signals (MDIO and MDC). It allows external devices with SMI master mode (MDC is output) to control the state of the PHY and internal registers (SMI slave mode: MDC is input). MDC is an input clock for the RTL8305SB Ver.D to latch MDIO on its rising edge. The clock can run from DC to 25MHz. MDIO is a bi-directional connection used to write data to, or read data from the RTL8305SB Ver.D. The PHY address is from 0 to 4.

Table 32. SMI Read/Write Cycles

	Preamble (32 bits)	Start (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1……..1	01	10	AAAAA	RRRRR	Z0	D…….D	Z*
Write	1……..1	01	01	AAAAA	RRRRR	10	D…….D	Z*

Z*: high-impedance. During idle time, MDIO state is determined by an external 1.5KΩ pull-up resistor.

The RTL8305SB Ver.D supports Preamble Suppression, which allows the MAC to issue Read/Write Cycles without preamble bits. However, for the first cycle of MII management after power-on reset, a 32-bit preamble is needed.

To guarantee the first successful SMI transaction after power-on reset, the external device should delay at least 1 second before issuing the first SMI Read/Write Cycle relative to the rising edge of reset.

7.3.6. Head-Of-Line Blocking

The RTL8305SB Ver.D incorporates an advanced mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8305SB Ver.D first checks the destination address of the incoming packet. If the destined port is congested, the RTL8305SB Ver.D will discard this packet to avoid blocking following packets that are destined for a non-congested port.

7.3.7. Port-Based VLAN and VLAN Tag Forwarding

The RTL8305SB Ver.D supports five VLAN groups: VLAN A, B, C, D, and E. Two association ingress rules are provided to map a frame to a given VLAN: port-based and tagged-VID (VLAN Identifier).

Port-based VLAN mapping is the simplest implicit mapping rule. A frame belongs to a VLAN based on the index of the port that it came from. P0VLANIndex[2:0], P1VLANIndex[2:0], P2VLANIndex[2:0], P3VLANIndex[2:0], and P4VLANIndex[2:0] are used for each port as the distinguishing characteristic of the particular VLAN. Using the default value as an example:

- P0VLANIndex[2:0]=0b000 means port0 belongs to VLAN A
- P1VLANIndex[2:0]=0b001 means port1 belongs to VLAN B
- P2VLANIndex[2:0]=0b010 means port2 belongs to VLAN C
- P3VLANIndex[2:0]=0b011 means port3 belongs to VLAN D
- P4VLANIndex[2:0]=0b100 means port4 belongs to VLAN E

The 12-bit tagged-VID is the explicit indication of the frame's VLAN association. A total of 4094 values are possible. The value of all ones (0xFFF) is reserved and currently unused. A value of all zeros (0x000) indicates a priority tag. A priority tagged frame is treated the same as an untagged frame. VIDA[11:0], VIDB[11:0], VIDC[11:0], VIDD[11:0], and VIDE[11:0] are used as the distinguishing characteristic for each VLAN. For example, VIDA[11:0]=0x001 means a frame with tagged-VID=0x001 belongs to VLAN A. VIDB[11:0]=0x002 means a frame with tagged-VID=0x002 belongs to VLAN B. VID fields have no default values in the register, users must assign them in the serial EEPROM or register via SMI for the tagged-VID application.

Table 33. 802.1Q VLAN Tag Frame Format

Bytes0~5	Bytes6~11	Bytes12~13	Bytes14.7~14.5	Byte14.4	Bytes14.3~15.0
DA	SA	V81-00	User-Priority (0~3:Low-pri; 4~7: High-pri)	CFI0	VID

For the egress rule, each VLAN has a Member Set field. The member set of a VLAN indicates which ports belong to this VLAN. Ports in the member set for a given VLAN can be expected to receive and transmit frames belonging to that VLAN; ports not in the member set should generally not be receiving and/or transmitting frames for that VLAN. For the RTL8305SB Ver.D, the member set for a VLAN can be configured by serial EEPROM or register via SMI. Using the default values as an example, MemberA[4:0]=10001 means port4 and 0 are members of VLAN A. MemberB[4:0]=10010 means port4 and 1 are

members of VLAN B. MemberC[4:0]=10100 means port4 and 2 are members of VLAN C. MemberD[4:0]=11000 means port4 and 3 are members of VLAN D. MemberE[4:0]=11111 means all ports are members of VLAN E.

When the serial EEPROM does not exist and pin DisVLAN=1, the RTL8305SB Ver.D will disable the VLAN function. The SMI can be used to update the registers; then do a SoftReset to enable and change the VLAN.

When the serial EEPROM does not exist and pin DisVLAN=0, the RTL8305SB Ver.D will use the default values for the internal register to provide a useful port-based VLAN mapping: P0VLANIndex[2:0]=0b000, P1VLANIndex[2:0]=0b001, P2VLANIndex[2:0]=0b010, P3VLANIndex[2:0]=0b011, and P4VLANIndex[2:0]=0b100; MemberA[4:0]=10001, MemberB[4:0]=10010, MemberC[4:0]=10100, MemberD[4:0]=11000, MemberE[4:0]=11111. Port0 to 3 will be set as different VLANs and share the overlapping port4. Users can use SMI to update the register, then do a SoftReset to change the VLAN configuration.

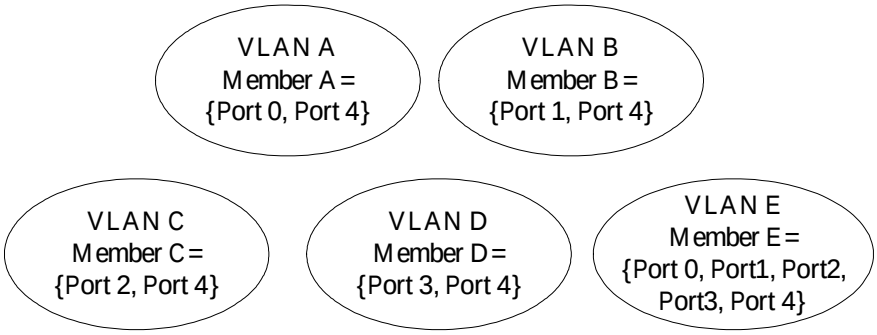


Figure 15. VLAN Configuration

Table 34. VLAN Configuration

	Port0	Port1	Port2	Port3	Port4
PortVLANIndex[2:0]	0b000 (VLAN A)	0b001 (VLAN B)	0b010 (VLAN C)	0b011 (VLAN D)	0b100 (VLAN E)

Table 35. 802.1Q VLAN Default Setup

	MemberA[4:0]	MemberB[4:0]	MemberC[4:0]	MemberD[4:0]	MemberE[4:0]
VLAN Member Reg.	0b10001	0b10010	0b10100	0b11000	0b11111
Port0	V				V
Port1		V			V
Port2			V		V
Port3				V	V
Port4	V	V	V	V	V

When an EEPROM is used, the RTL8305SB Ver.D will ignore the pin and will load the initial value of the internal registers with the EEPROM values.

When register DisVLAN=1, the RTL8305SB Ver.D disables the VLAN function. When register DisVLAN=0, the RTL8305SB Ver.D uses the internal register values to determine VLAN mapping.

If the 802.1Q tagged-VID Aware function is enabled (DisTagAware=0), the RTL8305SB Ver.D will check the tagged VID of the received frame to do the VLAN classification. The RTL8305SB Ver.D will use tagged-VID VLAN mapping for tagged frames and port-based VLAN mapping for untagged and priority-tagged frames. For example, when DisTagAware=0, if an untagged frame is received from port1 it will be classified as VLAN B when P1VLANIndex[2:0]=0b001 (i.e. port1 belongs to VLAN B). If a tagged frame with tagged-VID=0x001 is received from port1, it will be classified as VLAN A when VIDA[11:0]=0x001. If the tagged-VID Aware function is disabled, the RTL8305SB Ver.D will always use port-based VLAN mapping. For example, if a tagged frame with tagged-VID=0x001 is received from port1, it will be classified as VLAN B when P1VLANIndex[2:0]=0b001 (i.e. port1 belongs to VLAN B).

For flexible application, two ingress filtering options are available:

Ingress filtering option 1: The Acceptable Frame Type can be “Admit All” or “Admit All Tagged”. When DisTagAdmitCtrl=1, the Acceptable Frame Type of Ingress Process will be “Admit All” and the RTL8305SB Ver.D will receive all frames. When DisTagAdmitCtrl=0 and DisTagAware=0, the Acceptable Frame Type of Ingress Process will be “Admit All Tagged”. The RTL8305SB Ver.D will receive only the VLAN-tagged frame and drop all other untagged frames and priority tagged (VID=0) frames.

Ingress filtering option 2: When DisMemFilter=1, VLAN Ingress Member Set filtering is disabled. The RTL8305SB Ver.D will not discard any frames associated with a VLAN for which that port is not in the member set. If VLAN Ingress Member Set filtering is enabled by setting DisMemFilter=0, the RTL8305SB Ver.D will discard any frame associated with a VLAN for which that port is not in the member set.

In the first example, the RTL8305SB Ver.D will drop a frame received from port0 when DisVLAN=0, DisTagAware=1 (i.e. Port-Based VLAN), DisMemFilter=0, P0VLANIndex[1:0]=0b001 (i.e. port0 belongs to VLAN B), and MemberB[4:0]=0b10010 (i.e. port4 and 1 belong to the member set of VLAN B, as shown in the following figure). In the second example, RTL8305SB Ver.D will drop the frame with tagged-VID=0x002 received from port0 when DisVLAN=0, DisTagAware=0 (i.e. Tagged-VID VLAN mapping), DisMemFilter=0, VIDB[11:0]=0x002, and MemberB[4:0]=0b10010 (i.e. port4 and 1 belong to the member set of VLAN B, as shown in the following figure).

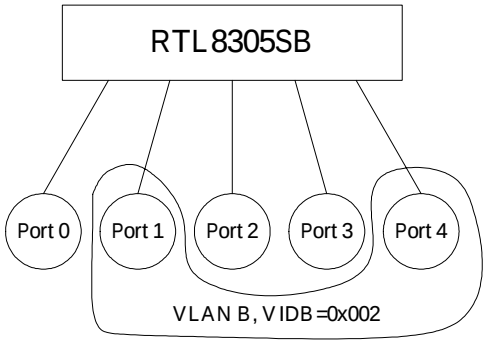


Figure 16. Example of VLAN Configuration for DisMemFilter

Example 1:

- P0VLANIndex=0b001 => Port0 belongs to VLAN B
- MemberB[4:0]=0b10010 => Members of VLAN B include Ports1 and 4

  Result: DisVLAN=0, DisTagAware=1, DisMemFilter=0, tagged or untagged packets from port0 will be discarded

Example 2:

- MemberB[4:0]=0b10010 => Members of VLAN B include Ports 1 and 4
- VIDB[11:0]=0x002 => Packets with tagged-VID=0x002 belong to VLAN B

  Result: DisVLAN=0, DisTagAware=0, DisMemFilter=0, tagged packets with VID=0x002 from port0 will be discarded

Two egress filtering options can be used for special applications:

Egress filtering option 1 (ARP VLAN): If DisARP=0, ARP broadcast frames (the RTL8305SB Ver.D only checks frames with DID=all F, Ether Type=0806, as shown in the following table) will be broadcast to all VLAN. Otherwise, ARP broadcast frames, like other frames, can only be forwarded to the same VLAN segment.

Table 36. ARP Frame Format

6 bytes	6 bytes	4 bytes	2 bytes	
All F	SA	802.1Q Tag (optional)	08-06	----

Egress filtering option 2 (Leaky VLAN): If DisLeaky=0, unicast frames with or without a tag, not including broadcast and multicast frames, can traverse VLAN segments. Otherwise, unicast frames can only be forwarded to the same VLAN segment. For example, as shown in the following figure, unicast frames from port0 can be forwarded to port3 if DisLeaky=0 (Port-Based VLAN). Tagged frames with VID=0x001 from port0 could also be forwarded to port3 if DisLeaky=0 and DisTagAware=0 (Tag-VID VLAN mapping).

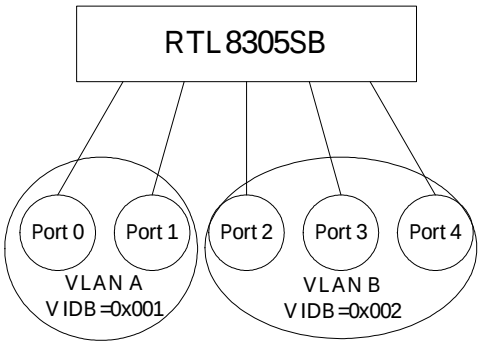


Figure 17. Example of VLAN Configuration for Leaky VLAN

7.3.8. QoS Function

The RTL8305SB Ver.D can recognize the QoS priority information of incoming packets to give a different egress service priority. The RTL8305SB Ver.D identifies the packets as high priority based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q VLAN priority tag
- TCP/IP's TOS/DiffServ (DS) priority field

The types of QoS are selected by hardware pins DisPortPri[4:0], DisTagPri, and DisDSPri respectively upon reset, or by internal registers via SMI after reset.

There are two priority queues, a high-priority queue and a low-priority queue. The queue service rate is based on the Weighted Round Robin algorithm, the packet-based service weight ratio of the high-priority queue and low-priority queue can be set to 4:1, 8:1, 16:1 or "Always high priority first" by hardware pins QWeight[1:0] upon reset, or internal register via SMI after reset.

When port-based priority is applied, packets received from the high-priority port, set by DisPortPri[4:0], will be sent to the high-priority queue of the destination port.

When 802.1p VLAN tag priority applies, the RTL8305SB Ver.D recognizes the 802.1Q VLAN tag frames and extracts the 3-bit User Priority information from the VLAN tag. The RTL8305SB Ver.D sets the threshold of User Priority as 3. Therefore, VLAN tagged frames with User Priority value = 4~7 will be treated as high priority frames, other User Priority values (0~3) as low priority frames (follows 802.1p standard).

When TCP/IP's TOS/DiffServ(DS) based priority is applied, the RTL8305SB Ver.D recognizes TCP/IP Differentiated Services Codepoint (DSCP) priority information from the DS-field defined in RFC2474. The DS field byte for the IPv4 is a Type-of-Service (TOS) octet and for IPv6 is a Traffic-Class octet. The recommended DiffServ Codepoint is defined in RFC2597 to classify the traffic into different service classes. The RTL8305SB Ver.D extracts the codepoint value of DS-fields from IPv4 and IPv6 packets, and identifies the priority of the incoming IP packet following the definition below:

High priority: where the DS-field = (EF, Expected Forwarding:) 101110
(AF, Assured Forwarding:) 001010; 010010; 011010; 100010
(Network Control:) 110000 and 111000

Low priority: where the DS-field = other values.

The VLAN tagged frame and 6-bit DS-field in the IPv4 and IPv6 frame format are shown below:

Table 37. 802.1Q VLAN Tag Frame Format

6 bytes	6 bytes	2 bytes	3 bits	
DA	SA	81-00	User-Priority (0~3:Low-pri ; 4~7: High-pri)	----

Table 38. IPv4 Frame Format

6 bytes	6 bytes	4 bytes	2 bytes	4 bits	4 bits	6 bits	
DA	SA	802.1Q Tag (optional)	08-00	Version IPv4= 0100	IHL	TOS[0:5]= DS-field	----

Table 39. IPv6 Frame Format

6 bytes	6 bytes	4 bytes	2 bytes	4 bits	6 bits	
DA	SA	802.1Q Tag (optional)	08-00	Version Ipv6= 0110	TOS[0:5]= DS-field	----

Note: IPv6 refer to rcf2460

The RTL8305SB Ver.D can be configured to turn off 802.3x flow control and back pressure flow control for 1~2 seconds whenever the port receives VLAN-tag or TOS/DS high priority frames. Flow control is re-enabled when no priority frame is

received for a 1~2 second duration. The hardware pin DisFCAutoOff upon reset, or internal register via SMI after reset, enables this auto turn off function.

7.3.9. Insert/Remove VLAN Priority Tag

When the QoS (Quality of Service) function is enabled, the RTL8305SB Ver.D can be configured to insert a VLAN priority-tag (VID=0x000) for untagged frames only, or remove the tag from all tagged frames, on a per output port basis. When the port is configured to Insert VLAN Priority Tag, content of already tagged frames won't be changed, but untagged frames will have a 4-byte priority tag inserted after the Source MAC Address field. Port4 can use two strapping pins upon reset, or internal registers via SMI after reset, to set the Insert/Remove function. Other ports can use a serial EEPROM upon reset, or internal registers via SMI after reset, to set this function. For example:

- When P0IRTag[1:0]=10, the RTL8305SB Ver.D inserts a priority tag on untagged frames from both the Output High Queue (user priority field=0b111, CFI=0, VID=0x000) of Port0 and the Low Queue of Port0 (user priority field=0b000, CFI=0, VID=0x000)
- When P0IRTag[1:0]=01, the RTL8305SB Ver.D inserts priority tags only on untagged frames from the Output High Queue of Port0 (user priority field=0b111, CFI=0, VID=0x000)
- If the tag removed frame is less than 64 bytes, it will be padded with an 0x20 pattern before the packet's CRC field to fit the 64-byte minimum packet length of the IEEE 802.3 spec. The RTL8305SB Ver.D will recalculate the FCS (Frame Check Sequence) if the frame has been changed.

7.3.10. Special Insert VLAN Tag

Table 40 shows the VLAN tag frame format of a standard Ethernet packet.

Table 40. VLAN Tag Frame Format

Bytes0~5	Bytes6~11	Bytes12~13	Bytes14.7~14.5	Byte14.4	Bytes14.3~15.0
DA	SA	81-00	User-Priority	CFI	VID

When any port of the RTL8305SB Ver.D is configured to enable the insert VLAN tag function, the switch will insert a 4-byte VLAN tag after the SA of the packet, as shown in Table 41.

Table 41. Insert VLAN Tag Frame Format

Bytes0~5	Bytes6~11	Bytes12~13	Bytes14.7~14.5	Byte14.4	Bytes14.3~15.0
DA	SA	81-00	User-Priority 0:Low-pri queue 7: High-pri queue	CFI 0	VID 0

When the special insert VLAN tag function is enabled (**P4IRTag[1:0]=01 and DisSpecialTag=0**), high priority packets that do not have a VLAN tag will have a tag inserted in the frame format as shown in Table 42 (Type I). Byte 12~13 of the frame will be inserted ***8101h***, Priority be ***7h***, CFI be ***0h***, and VID be ***0h*** (priority tag packet).

Table 42. Insert VLAN Tag Frame Format for High Priority Queue Type I

Bytes0~5	Bytes6~11	Bytes12~13	Bytes14.7~14.5	Byte14.4	Bytes14.3~15.0
DA	SA	81-01	User-Priority 7: High-pri queue	CFI 0	VID 0

High priority packets that already have a VLAN tag will have the tag replaced as shown in the frame format shown in Table 43 (Type II). Byte 12~13 of the frame will be replaced by ***8102h***, Priority, CFI, and VID fields will be the same as the original packet.

Table 43. Insert VLAN Tag Frame Format for High Priority Queue Type II

Bytes0~5	Bytes6~11	Bytes12~13	Bytes14.7~14.5	Byte14.4	Bytes14.3~15.0
DA	SA	81-02	User-Priority X (No Change)	CFI X (No Change)	VID X (No Change)

7.3.11. Filtering/Forwarding Reserved Control Frame

The RTL8305SB Ver.D supports the ability to forward or drop the frames of the 802.1D specified reserved group MAC addresses (control frames): 01-80-C2-00-00-03 to 01-80-C2-00-00-0F.

Table 44. EnForward=1

Address	Use	Action
01-80-C2-00-00-00	Bridge Group Address	Forward to all ports
01-80-C2-00-00-01	Pause Control Frame	Drop Frame
01-80-C2-00-00-02		Drop Frame
01-80-C2-00-00-03 to 01-80-C2-00-00-0F	Reserved	Forward to all ports
Any other multicast Address	-	Forward to all ports

Table 45. EnForward=0

Address	Use	Action
01-80-C2-00-00-00	Bridge Group Address	Forward to all ports
01-80-C2-00-00-01	Pause Control Frame	Drop Frame
01-80-C2-00-00-02		Drop Frame
01-80-C2-00-00-03 to 01-80-C2-00-00-0F	Reserved	Drop Frame
Any other multicast Address	-	Forward to all ports

7.3.12. Broadcast Storm Control

According to the latched value of the DISBRDCTRL pin upon reset, the RTL8305SB Ver.D determines whether or not to proceed with broadcast storm control. Once enabled (DISBRDCTRL=0), after 64 consecutive broadcast packets (DID=FFFF-FFFF-FFFF) are received by a particular port, the following incoming broadcast packets will be discarded by this port for approximately 800ms. Any non-broadcast packet can reset the time window and broadcast counter such that the scheme restarts.

Note: Trigger condition: consecutive 64 DID = FFFF-FFFF-FFFF packets. Release condition: receive non-broadcast packet on or after 800ms.

7.3.13. Broadcast In/Out Drop

If some destination ports are blocking and the buffer is full, broadcast frames are dropped according to configuration.

1. Input Drop: Do not forward to any port and drop the frame directly
2. Output Drop: Forward only to non-blocking ports (Broadcast becomes multicast)

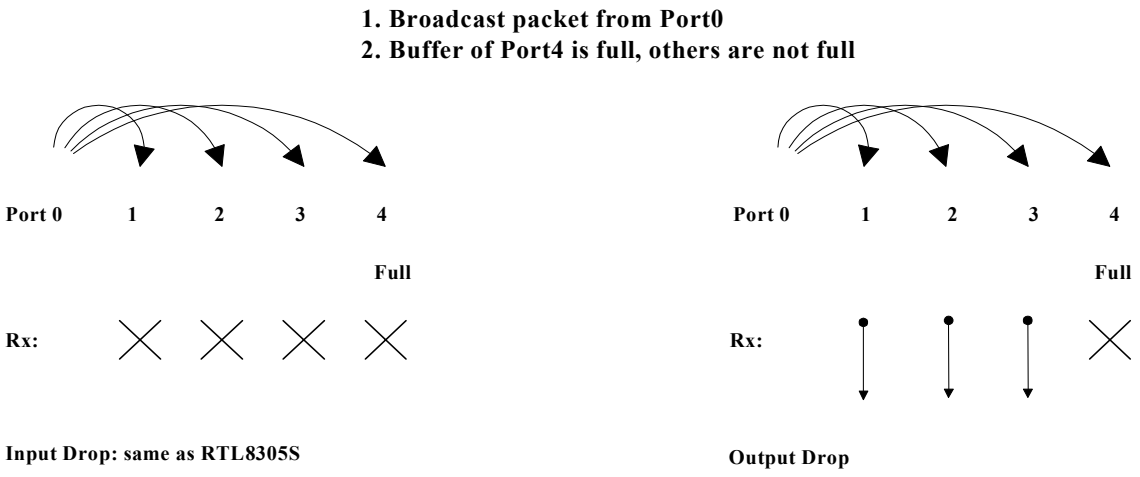


Figure 18. Input Drop vs. Output Drop

7.3.14. Loop Detection

Loops should be avoided between switch applications. The simplest loop as shown below results in: 1) Unicast frame duplication; 2) Broadcast frame multiplication; 3) Address table nonconvergence. Frames may be transmitted from Switch1 to Switch2 via Link1, then returned to Switch1 via Link2.

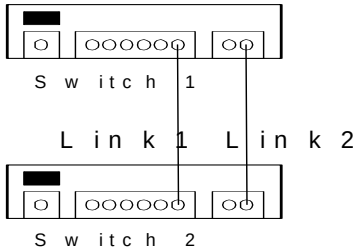


Figure 19. Loop Example

When the loop detection function is enabled by setting DisLoop=0 in EEPROM or an internal register, the RTL8305SB Ver.D periodically sends out a broadcast 64-byte packet every 3~5 minutes and automatically detects whether there is a network loop (or bridge loop). If a loop is detected the LoopLED# will be ON (active low or high). The LED goes out when both RTL8305SB Ver.D ports of the loop are unplugged. The Loop frame length is 64 bytes and its format is shown below.

Table 46. Loop Frame Format

FFFF FFFF FFFF	SID	8899	0300 000…0000	CRC

In order to achieve loop detection, each switch device needs a unique SID (the source MAC address). If the EEPROM is not used, a unique SID should be assigned via SMI after reset, and the default SID (0x52 54 4c83 05 b0) should not be used.

Ethernet MAC address byte (bit) ordering: For example, if the MAC address is 52 54 4c 00 01 02, according to 802.3, 0x52 should be byte 0, 0x54 is byte 1, etc.

Table 47. Ethernet MAC Address Ordering

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
HEX	52	54	4c	00	01	02
Bits	0101 0010	0101 0100	0100 1100	0000 0000	0000 0001	0000 0010
	Bit7~0	Bit15~8	Bit23~16	Bit31~24	Bit39~32	Bit47~40

7.3.15. MAC Loopback Return to External

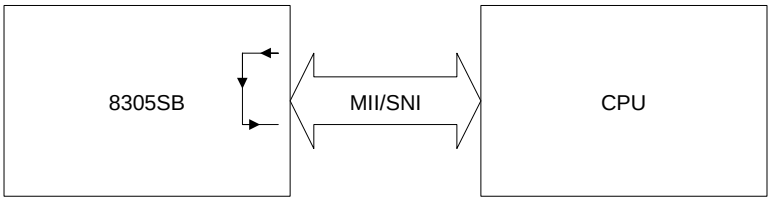
Each port supports loopback of the MAC (return to external device) function for diagnostic purposes.

Example 1: If the internal register DisP4LoopBack=0, the RTL8305SB Ver.D will "forward local and broadcast packets from the input of Port4 to the output of Port4" and "drop unicast packets from the input of Port4". Other ports can still forward broadcast or unicast packets to port4.

Example 2: If the internal register DisP3LoopBack=0, the RTL8305SB Ver.D will "forward local and broadcast packets from the input of Port3 to the output of Port3" and "drop unicast packets from the input of Port3". Other ports can still forward broadcast or unicast packets to port3.

This is especially useful for router applications performing mass production tests. This function is independent of PHY type (GxMode/GyMode/P4Mode[1:0]) and can be done on each mode. Below are two examples: In Example 1 the external device (CPU) is connected to the MII or SNI interface of Port4. In Example 2, the external device (CPU) does not have an MII or SNI interface, so it uses the PCI interface to connect an RTL8139 to the UTP of Port4.

Example 1: LoopBack in external PHY mode



Example 2: LoopBack in UTP mode

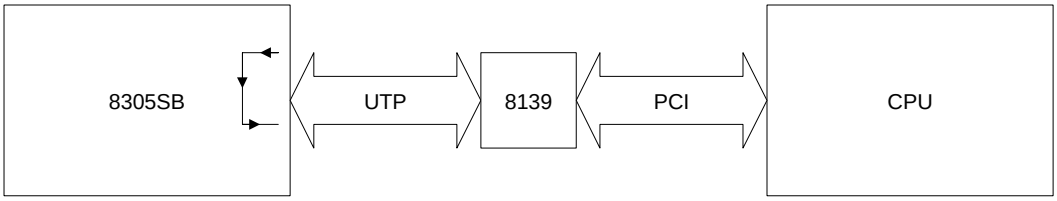


Figure 20. Port4 Loopback

7.3.16. Reg0.14 PHY Loopback Return to Internal

The loopback mode of the PHY (return to internal MAC) may be enabled on a per port basis by setting MII Reg.0.14 to 1. In Reg0.14 loopback mode, the TXD of PHY is transferred directly to the RXD of PHY with TXEN changed to CRS_DV, and returns to MAC via an internal MII. The data stream coming from the MAC will not egress to the physical medium and an incoming data stream from the network medium will be blocked in this mode. The packets will be looped back in 10Mbps full duplex or 100Mbps full duplex mode. This function is especially useful for diagnostic purposes. For example, a NIC can be used to send broadcast frames into port0 of the RTL8305SB Ver.D and set Port1 to Reg0.14 Loopback. The frame will be looped back to port0, so the received packet count can be checked to verify that the switch device is good. In this example, port0 can be 10M or 100M and full or half duplex.

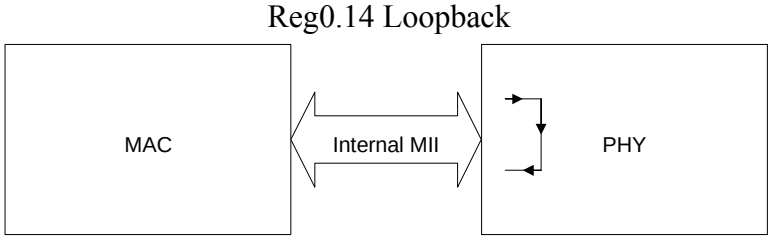


Figure 21. Reg.0.14 Loopback

7.3.17. LEDs

The RTL8305SB Ver.D supports four parallel LEDs for each port, and two special LEDs (SELMIIMAC# and LOOPLED#). Each port has four LED indicator pins. Each pin may have different indicator meanings set by pins LEDMode[1:0]. Refer to the pin descriptions for details (Port LED Pins, on page 14). Upon reset, the RTL8305SB Ver.D supports chip diagnostics and LED functions by blinking all LEDs once for 320ms. This function can be disabled by asserting EN_RST_LINK to 0. LED_BLINK_TIME determines the LED blinking period for activity and collision (1 = 43ms and 0 = 120ms). The parallel LEDs corresponding to port4 can be three-stated (disable LED functions) for MII port application by setting ENP4LED in EEPROM to 0. In UTP applications, this bit should be set to 1.

All LED pins are dual function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is floating upon reset, the pin output is active low after reset. Otherwise, if the pin input is pulled down upon reset, the pin output is active high after reset. Exception: Bi-color Link/Act mode of pin LED_ADD[4:0] when LEDMode[1:0]=10. Below is an example circuit for LEDs. The typical values for pull-down resistors are 10K Ω.

Figure 22. Floating and Pull-Down of LED Pins

For two pin Bi-color LED mode (LEDMode[1:0]=10), Bi-color Link/Act (pin LED_ADD) and Spd (pin LED_SPD) can be used for one Bi-color LED package, which is a single LED package with two LEDs connected in parallel with opposite polarity. When LEDMode[1:0]=10, the active status of LED_ADD is the opposite of LED_SPD.

Table 48. Spd and Bi-color Link/Act Truth Table

		Spd:Input=Floating, Active Low. Bi-color Link/Act: the active status of LED_ADD is the opposite of LED_SPD and does not interact with input upon reset.		**Spd:Input=Pull-down, Active High. Bi-color Link/Act:** the active status of LED_ADD is the opposite of LED_SPD and does not interact with input upon reset.	
Indication	**Bi-Color State**	**Spd**	**Link/Act**	**Spd**	**Link/Act**
No Link	Both Off	1	1	0	0
100M Link	Green On	0	1	1	0
10M Link	Yellow On	1	0	0	1
100M Act	Green Flash	0	Flash	1	Flash
10M Act	Yellow Flash	1	Flash	0	Flash

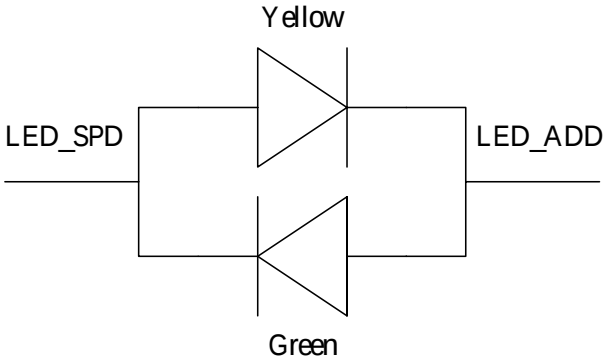


Figure 23. Two Pin Bi-color LED for SPD Floating or Pull-high

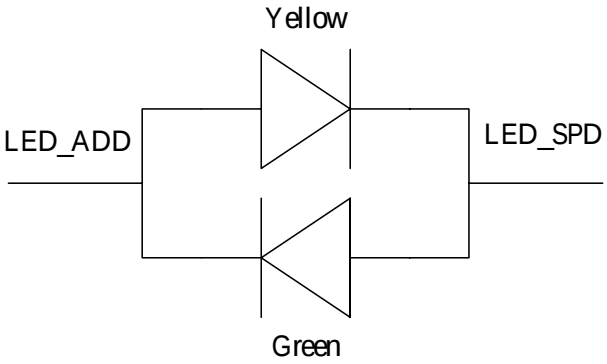


Figure 24. Two Pin Bi-color LED for SPD Pull-down

7.3.18. 2.5V Power Generation

The RTL8305SB Ver.D can use a PNP transistor to generate 2.5V from a 3.3V power supply. This 2.5V is used for the digital core and analog receiver circuits. Do not use one PNP transistor for more than one RTL8305SB Ver.D chip, even if the rating is enough.

Do not connect an inductor (bead) directly between the collector of the PNP transistor and RVDD. This will adversely affect the stability of the 2.5V power significantly.

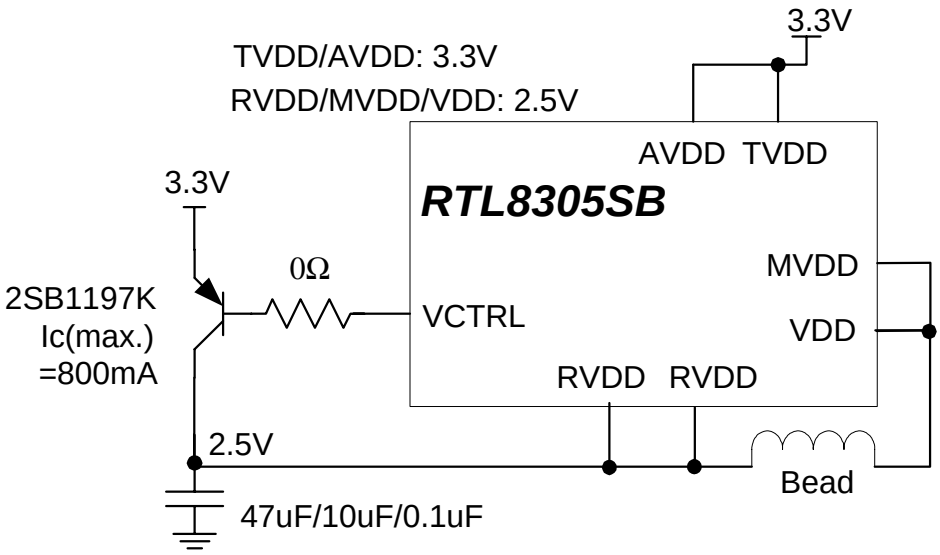


Figure 25. Using a PNP Transistor to Transform 3.3V Into 2.5V

Table 49. An Example Using Power Transistor 2SB1197K

Parameter	Symbol	Limits	Unit
Collector-base voltage	VCBO	-40	V
Collector-emitter voltage	VCEO	-32	V
Emitter-base voltage	VEBO	-5	V
Collector current	IC	-0.8	A(DC)
Collector power dissipation	PC	0.2	W
Junction temperature	Tj	150	°C
Storage temperature	Tstg	-55~+150	°C

Absolute maximum ratings (Ta=25°C)
For more information, refer to http://www.rohm.com

7.3.19. Crystal/Oscillator

The frequency is 25Mhz. The maximum Frequency Tolerance is +/- 50ppm. The maximum Jitter is 150ps Peak-to-Peak.

8. Serial EEPROM Description

Unused Registers and bits are reserved for future or internal use, and should use the default value.

Table 50. Serial EEPROM Description

Name	Reg.bit	PHY Reg. Mapping	Description	Default
Internal	0.7	PHY0, Reg.16.7	Internal use only	1b
Internal	0.6	PHY0, Reg.16.6	Internal use only	1b
Internal	0.5	PHY0, Reg.16.5	Internal use only	1b
Internal	0.4	PHY0, Reg.16.4	Internal use only	1b
Internal	0.3	PHY0, Reg.16.3	Internal use only	1b
Internal	0.2	PHY0, Reg.16.2	Internal use only	1b
Internal	0.1	PHY0, Reg.16.1	Internal use only	1b
NoEEPROM	0.0	PHY0, Reg.16.0	**No EEPROM:** 1: EEPROM does not exist 0: EEPROM exists	0b
Internal	1.7	PHY0, Reg.16.15	Internal use only	1b
DisLoop	1.6	PHY0, Reg.16.14	**Disable Loop Detection Function:** 1: Disable Loop Detection function 0: Enable Loop Detection function	1b
Internal	1.5	PHY0, Reg.16.13	Internal use only	1b
Internal	1.4	PHY0, Reg.16.12	Internal use only	1b
EnP4LED	1.3	PHY0, Reg.16.11	**Enable Port4 LED:** 1: Drive LED pins of port4 0: Do not drive LED pins of port4 for special application In UTP applications, this bit should be 1 to drive the LEDs of port4.	1b
Reserved	1.2	PHY0, Reg.16.10		1b
Reserved	1.1	PHY0, Reg.16.9		1b
Reserved	1.0	PHY0, Reg.16.8		1b
Reserved	2.7~2.4	PHY0, Reg.17.7~4		1111b
Internal	2.3~2.0	PHY0, Reg.17.3~0	Internal use only	0000b
Reserved	3.7~3.2	PHY0, Reg.17.15~10		1
Internal	3.1~3.0	PHY0, Reg.17.9~8	Internal use only	11
EthernetID	4~9	4: PHY0, Reg.18.7~0 5: PHY0, Reg.18.15~8 6: PHY0, Reg.19.7~0 7: PHY0, Reg.19.15~8 8: PHY0, Reg.20.7~0 9: PHY0, Reg.20.15~8	**Device Ethernet MAC ID (6 bytes).** Example: for MAC ID = 52 54 4C 83 05 B0. Byte4 = 0x52 (Byte 1 of MAC ID) Byte5 = 0x54 (Byte 2 of MAC ID) Byte6 = 0x4C (Byte 3 of MAC ID) Byte7 = 0x83 (Byte 4 of MAC ID) Byte8 = 0x05 (Byte 5 of MAC ID) Byte9 = 0xB0 (Byte 6 of MAC ID)	52h 54h 4Ch 83h 05h B0h
Reserved	10.7	PHY0, Reg.21.7		1b
P1VLANIndex[2] P1VLANIndex[1] P1VLANIndex[0]	10.6 10.5 10.4	PHY0, Reg.21.6 PHY0, Reg.21.5 PHY0, Reg.21.4	**Port1 VLAN Index:** P1VLANIndex[2:0]=001 means port1 uses the second VLAN (VLAN B).	001b
Reserved	10.3	PHY0, Reg.21.3		1b
P0VLANIndex[2] P0VLANIndex[1] P0VLANIndex[0]	10.2 10.1 10.0	PHY0, Reg.21.2 PHY0, Reg.21.1 PHY0, Reg.21.0	**Port0 VLAN Index:** P0VLANIndex[2:0] is used to assign the VLAN of port0. For example, P0VLANIndex[2:0]=000 means port0 uses the first VLAN (VLAN A). P0VLANIndex[0] is bit0, P0VLANIndex[1] is bit1, P0VLANIndex[2] is bit2.	000b
Reserved	11.7	PHY0, Reg.21.15		1b

Name	Reg.bit	PHY Reg. Mapping	Description	Default
P3VLANIndex[2] P3VLANIndex[1] P3VLANIndex[0]	11.6 11.5 11.4	PHY0, Reg.21.14 PHY0, Reg.21.13 PHY0, Reg.21.12	**Port3 VLAN Index:** P3VLANIndex[2:0]=011 means port3 use the fourth VLAN (VLAN D).	011b
Reserved	11.3	PHY0, Reg.21.11		1b
P2VLANIndex[2] P2VLANIndex[1] P2VLANIndex[0]	11.2 11.1 11.0	PHY0, Reg.21.10 PHY0, Reg.21.9 PHY0, Reg.21.8	**Port2 VLAN Index:** P2VLANIndex[2:0]=010 means port2 use the third VLAN (VLAN C).	010b
Reserved	12.7~12.3	PHY0, Reg.22.7~3		11111b
P4VLANIndex[2] P4VLANIndex[1] P4VLANIndex[0]	12.2~12.0	PHY0, Reg.22.2~0	**Port4 VLAN Index:** P4VLANIndex[2:0]=100 means port4 use the fifth VLAN (VLAN E).	100b
P3IRTag[1] P3IRTag[0]	13.7 13.6	PHY0, Reg.22.15 PHY0, Reg.22.14	**Insert/Remove Priority Tag of Port3:** 11: Do not insert/remove Tag from Output High and Low Queue of Port3. 10: Insert Tag from Output High and Low Queue of Port3. 01: Insert Tag from Output High Queue only of Port3. 00: Remove Tag from Output High and Low Queue of Port3.	11b
P2IRTag[1] P2IRTag[0]	13.5 13.4	PHY0, Reg.22.13 PHY0, Reg.22.12	**Insert/Remove Priority Tag of Port2:** 11: Do not insert/remove Tag from Output High and Low Queue of Port2. 10: Insert Tag from Output High and Low Queue of Port2. 01: Insert Tag from Output High Queue only of Port2. 00: Remove Tag from Output High and Low Queue of Port2.	11b
P1IRTag[1] P1IRTag[0]	13.3 13.2	PHY0, Reg.22.11 PHY0, Reg.22.10	**Insert/Remove Priority Tag of Port1:** 11: Do not insert/remove Tag from Output High and Low Queue of Port1. 10: Insert Tag from Output High and Low Queue of Port1. 01: Insert Tag from Output High Queue only of Port1. 00: Remove Tag from Output High and Low Queue of Port1.	11b
P0IRTag[1] P0IRTag[0]	13.1 13.0	PHY0, Reg.22.9 PHY0, Reg.22.8	**Insert/Remove Priority Tag of Port0:** 11: Do not insert/remove Tag from Output High and Low Queue of Port0. 10: Insert Tag from Output High and Low Queue of Port0. 01: Insert Tag from Output High Queue only of Port0. 00: Remove Tag from Output High and Low Queue of Port0.	11b
Internal	14~17	14: PHY1, Reg.16.7~0 15: PHY1, Reg.16.15~8 16: PHY1, Reg.17.7~0 17: PHY1, Reg.17.15~8	Internal use only	FFh FFh FFh FFh
Internal	18~21	18: PHY1, Reg.18.7~0 19: PHY1, Reg.18.15~8 20: PHY1, Reg.19.7~0 21: PHY1, Reg.19.15~8	Internal use only	FFh FFh FFh FFh

Name	Reg.bit	PHY Reg. Mapping	Description	Default
Internal	22~25	22: PHY1, Reg.20.7~0 23: PHY1, Reg.20.15~8 24: PHY1, Reg.21.7~0 25: PHY1, Reg.21.15~8	Internal use only	FFh FFh FFh FFh
Internal	26~29	26: PHY1, Reg.22.7~0 27: PHY1, Reg.22.15~8 28: PHY1, Reg.23.7~0 29: PHY1, Reg.23.15~8	Internal use only	FFh FFh FFh FFh
VIDA[11:0]	31.3~31.0 30.7~30.0	PHY1, Reg.24.11~8 PHY1, Reg.24.7~0	**VLAN Identifier of VLAN A:** Reg31.3=VIDA[11], Reg30.0=VIDA[0].	001h
Reserved	31.7~31.4	PHY1, Reg.24.15~12		1111b
Reserved	32.7~32.5	PHY1, Reg.25.7~5		111b
MemberA[4:0]	32.4~32.0	PHY1, Reg.25.4~0	**Member Set of VLAN A:** MemberA[4:0] determines the VLAN members of VLAN A. MemberA[4:0]=10001 means port4 and port0 are the members of VLAN A. MemberA[4:0]=10010 means port4 and port1 are the members of VLAN A. MemberA[4:0]=11111 means all ports are members of VLAN A.	10001b
VIDB[11:0]	34.3~34.0 33.7~33.0	PHY1, Reg.26.3~0 PHY1, Reg.25.15~8	**VLAN Identifier of VLAN B:**	002h
Reserved	34.7~34.4	PHY1, Reg.26.7~4		1111b
Reserved	35.7~35.5	PHY1, Reg.26.15~13		111b
MemberB[4:0]	35.4~35.0	PHY1, Reg.26.12~8	**Member Set of VLAN B:** MemberB[4:0]=10010 means port4 and port1 are the members of VLAN B.	10010b
VIDC[11:0]	37.3~37.0 36.7~36.0	PHY1, Reg.27.11~8 PHY1, Reg.27.7~0	**VLAN Identifier of VLAN C:**	003h
Reserved	37.7~37.4	PHY1, Reg.27.15~12		1111b
Reserved	38.7~38.5	PHY1, Reg.28.7~5		111b
MemberC[4:0]	38.4~38.0	PHY1, Reg.28.4~0	**Member Set of VLAN C:** MemberC[4:0]=10100 means port4 and port2 are the members of VLAN C.	10100b
VIDD[11:0]	40.3~40.0 39.7~39.0	PHY1, Reg.29.3~0 PHY1, Reg.28.15~8	**VLAN Identifier of VLAN D:**	004h
Reserved	40.7~40.4	PHY1, Reg.29.7~4		1111b
Reserved	41.7~41.5	PHY1, Reg.29.15~13		111b
MemberD[4:0]	41.4~41.0	PHY1, Reg.29.12~8	**Member Set of VLAN D:** MemberD[4:0]=11000 means port4 and port3 are the members of VLAN D.	11000b
VIDE[11:0]	43.3~43.0 42.7~42.0	PHY1, Reg.30.11~8 PHY1, Reg.30.7~0	**VLAN Identifier of VLAN E:**	005h
Reserved	43.7~43.4	PHY1, Reg.30.15~12		1111b
Reserved	44.7~44.5	PHY1, Reg.31.7~5		111b
MemberE[4:0]	44.4~44.0	PHY1, Reg.31.4~0	**Member Set of VLAN E:** MemberE[4:0]=11111 means all ports are members of VLAN E.	11111b
DisSpecialTag	45.7	PHY2, Reg.17.7	**Enable Special VLAN Tagging:** 1: Disable 0: Enable	1b
Internal	45.7	PHY2, Reg.17.6	Internal use only	1b

Name	Reg.bit	PHY Reg. Mapping	Description	Default
DisVLAN	45.5	PHY2, Reg.17.5	**Disable VLAN:** 1: Disable VLAN. 0: Enable VLAN. This register has higher priority than pin settings.	1b
DisTagAware	45.4	PHY2, Reg.17.4	**Disable Tag Aware:** 1: Disables the 802.1Q tagged-VID Aware function. The RTL8305SB Ver.D will not check the tagged VID of a received frame to do VLAN classification. The RTL8305SB Ver.D will always use Port-Based VLAN mapping. 0: Enables the Member Set Filtering function of the VLAN Ingress Rule. The RTL8305SB Ver.D will check the tagged VID of received frames to do VLAN classification. The RTL8305SB Ver.D will use tagged-VID VLAN mapping for tagged frames and will use Port-Based VLAN mapping for untagged and priority-tagged frames.	1b
DisMemFilter	45.3	PHY2, Reg.17.3	**Disable Member Set Filtering:** 1: Disable the Member Set Filtering function of the VLAN Ingress Rule. The RTL8305SB Ver.D will not discard any frames associated with a VLAN for which that port is not in the member set. 0: Enable the Member Set Filtering function of the VLAN Ingress Rule. The RTL8305SB Ver.D will discard any frames associated with a VLAN for which that port is not in the member set.	1b
DisTagAdmitCtrl	45.2	PHY2, Reg.17.2	**Disable Tag Admit Control: (Covers Acceptable Frame Type)** 1: Disable Tag Admit Control: Acceptable Frame Type is “Admit All”. The RTL8305SB Ver.D will receive all frames. 0: Enable Tag Admit Control: Acceptable Frame Type is “Admit All Tagged”. The RTL8305SB Ver.D will receive only VLAN-tagged frames and drop all other untagged frames and priority tagged (VID=0) frames.	1b
DisLeaky	45.1	PHY2, Reg.17.1	**Disable Leaky VLAN:** 1: Disable forwarding of unicast frames to other VLANs. 0: Enable forwarding of unicast frames to other VLANs. Broadcast and multicast frames adhere to the VLAN configuration. This register has higher priority than pin settings.	1b
DisARP	45.0	PHY2, Reg.17.0	**Disable ARP broadcast to all VLAN:** 1: Disable to broadcast the ARP broadcast packet to all VLANs. 0: Enable to broadcast the ARP broadcast packet to all VLANs. ARP broadcast frame: DID is all F. This register has higher priority than pin settings.	1b
Reserved	46.7	PHY3, Reg.17.7		1b

Name	Reg.bit	PHY Reg. Mapping	Description	Default
Internal	46.6	PHY3, Reg.17.6	Internal use only	1b
Internal	46.5~46.3	PHY3, Reg.17.5~3	Internal use only	000b
Internal	46.2~46.0	PHY3, Reg.17.2~0	Internal use only	100b
Internal	47.7~47.0 48.7~48.0 49.7~49.0 50.7~50.0 51.7~51.0 52.7~52.0	PHY3, Reg.18.7~0 PHY3, Reg.18.15~8 PHY3, Reg.19.7~0 PHY3, Reg.19.15~8 PHY3, Reg.20.7~0 PHY3, Reg.20.15~8	Internal use only	52h 54h 4C 83h 05h B1h

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 51. Electrical Characteristics/Ratings

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Vcc Supply Referenced to GND	-0.5	+4.0	V
Digital Input Voltage	-0.5	VDD	V
DC Output Voltage	-0.5	VDD	V

9.2. Operating Range

Parameter	Min	Max	Units
Ambient Operating Temperature (Ta)	0	+70	°C
3.3V Vcc Supply Voltage Range (AVDD, TVDD)	3.15	3.45	V
2.5V Vcc Supply Voltage Range (MVDD, RVDD, VDD)	2.375	2.625	V

9.3. DC Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
Power Supply Current for 2.5V	Icc	10Base-T, idle	55	60	65	mA
		10Base-T, Peak continuous 100% utilization	55	60	65	
		100Base-TX, idle	85	90	95	
		100Base-TX, Peak continuous 100% utilization	125	130	135	
		Power saving	55	60	65	
		Power down	55	60	65	
Power Supply Current for 3.3V	Icc	10Base-T, idle	45	50	55	mA
		10Base-T, Peak continuous 100% utilization	305	310	315	
		100Base-TX, idle	175	180	185	
		100Base-TX, Peak continuous 100% utilization	185	190	195	
		Power saving	25	30	35	
		Power down	25	30	35	
Total Power Consumption for all Ports	PS	10Base-T, idle	286	315	344	mW
		10Base-T, Peak continuous 100% utilization	1144	1173	1202	
		100Base-TX, idle	790	819	848	
		100Base-TX, Peak continuous 100% utilization	923	952	981	
		Power saving	220	249	278	
		Power down	220	249	278	
TTL Input High Voltage	V_{ih}		1.5			V
TTL Input Low Voltage	V_{il}				1.0	V
TTL Input Current	I_{in}		-10		10	uA
TTL Input Capacitance	C_{in}			3		pF
Output High Voltage	V_{oh}		2.25			V
Output Low Voltage	V_{ol}				0.4	V
Output Three State Leakage Current	$\|I_{OZ}\|$				10	uA

Parameter	SYM	Condition	Min	Typical	Max	Units
Transmitter, 100Base-TX (1:1 Transformer Ratio)						
TX+/- Output Current High	I_{OH}				20	mA
TX+/- Output Current Low	I_{OL}		0			uA
Transmitter, 10Base-T(1:1 Transformer Ratio)						
TX+/- Output Current High	I_{OH}				50	mA
TX+/- Output Current Low	I_{OL}		0			uA
Receiver, 100Base-TX						
RX+/- Common-mode Input Voltage				1.6		V
RX+/- Differential Input Resistance				20		kΩ
Receiver, 10Base-T						
Differential Input Resistance				20		kΩ
Input Squelch Threshold				340		mV

9.4. AC Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
Transmitter, 100Base-TX						
Differential Output Voltage, peak-to-peak	V_{OD}	50Ω from each output to Vcc, Best-fit over 14 bit times	0.970	0.990	1.030	V
Differential Output Voltage Symmetry	V_{OS}	50Ω from each output to Vcc, |Vp+|/ |Vp-|	98.4	100	101.6	%
Differential Output Overshoot	V_{OO}	Percent of Vp+ or Vp-	3.0	3.75	4.5	%
Rise/Fall time	t_r ,t_f	10-90% of Vp+ or Vp-	3.5	4.0	4.5	ns
Rise/Fall time imbalance	$\|t_r - t_f\|$		0	0.35	0.5	ns
Duty Cycle Distortion		Deviation from best-fit time-grid, 010101 … Sequence	15.5	16.0	16.5	ns
Timing jitter		Idle pattern	0.56	0.72	0.98	ns
Transmitter, 10Base-T						
Differential Output Voltage, peak-to-peak	V_{OD}	50Ω from each output to Vcc, all pattern	2.30	2.36	2.42	V
TP_IDL Silence Duration		Period of time from start of TP_IDL to link pulses or period of time between link pulses	10.72	13.0	15.75	ms
TD Short Circuit Fault Tolerance		Peak output current on TD short circuit for 10 seconds.	150	180	210	mA
TD Differential Output Impedance (return loss)		Return loss from 5MHz to 10MHz for reference resistance of 100 Ω	24.0	24.5	25.0	dB
TD Common-Mode Output Voltage	Ecm	Terminate each end with 50Ω resistive load	35	42	48	mV
Transmitter Output Jitter			6.8	7.4	8.0	ns
RD Differential Output Impedance (return loss)		Return loss from 5MHz to 10MHz for reference resistance of 100 Ω	24.0	24.5	25.0	dB
Harmonic Content		dB below fundamental, 20 cycles of all ones data	28	30	32	dB
Start-of-idle Pulse width		TP_IDL width	300	350	400	ns

9.5. Digital Timing Characteristics

Table 52. Digital Timing Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
100Base-TX Transmit System Timing						
Active TX_EN Sampled to first bit of "J" on MDI output				11	12	Bits
Inactive TX_EN Sampled to first bit of "T" on MDI output				15	16	Bits
TX Propagation Delay	tTXpd	From TXD[1:0] to TXOP/N		11	12	Bits
100Base-TX Receive System Timing						
First bit of "J" on MDI input to CRS_DV assert		From RXIP/N to CRS_DV		6	8	Bits
First bit of "T" on MDI input to CRS_DV de-assert		From RXIP/N to CRS_DV		16	18	Bits
RX Propagation Delay	tRXpd	From RXIP/N to RXD[1:0]		15	17	Bits
10Base-T Transmit System Timing						
TX Propagation Delay	tTXpd	From TXD[1:0] to TXOP/N		5	6	Bits
TXEN to MDI output		From TXEN assert to TXOP/N		5	6	Bits
10Base-T Receive System Timing						
Carrier Sense Turn-on delay	tCSON	Preamble on RXIP/N to CRS_DV asserted		12		Bits
Carrier Sense Turn-off Delay	tCSOFF	TP_IDL to CRS_DV de-asserted		8	9	Bits
RX Propagation Delay	tRXpd	From RXIP/N to RXD[1:0]	9		12	Bits
LED Timing						
LED On Time	tLEDon	While LED blinking	43		120	ms
LED Off Time	tLEDoff	While LED blinking	43		120	ms

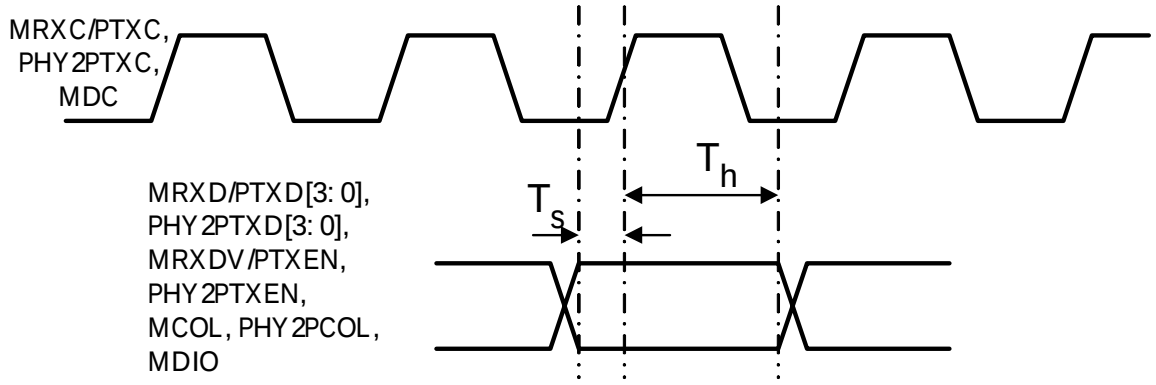


Figure 26. Reception Data Timing of MII/SNI/SMI Interface

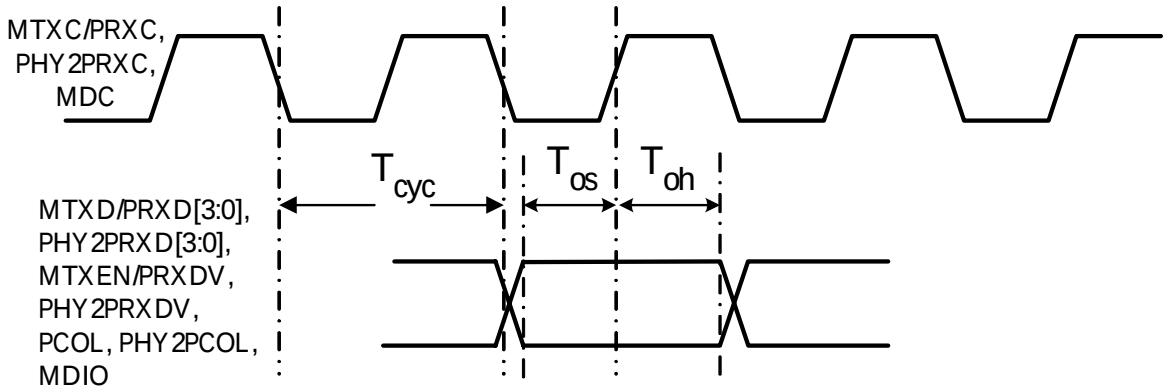


Figure 27. Transmission Data Timing of MII/SNI/SMI Interface

Table 53. MII & SMI DC Timing

Parameter	SYM	Condition	I/O	Min	Type	Max	Units
MAC Mode MII Timing (DISINVERTER is pulled high)							
100BaseT MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC clock cycle time	I		40±50 ppm		ns
10BaseT MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC clock cycle time	I		400±50 ppm		ns
MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV Output Setup time	T_{os}	Output Setup time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV	O	22	24	26	ns
MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV Output Hold time	T_{oh}	Output Hold time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV	O	14	16	18	ns
MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN, MCOL/PCOL Setup time	T_s	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge setup time	I	4			ns
MRXD/PTXD, MRXDV/PTXEN, MCOL/PCOL Hold time	T_h	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge hold time	I	2			ns

Parameter	SYM	Condition	I/O	Min	Type	Max	Units
PHY Mode MII Timing (DISINVERTER is pulled high)							
100BaseT MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC clock cycle time	O		40±50 ppm		ns
10BaseT MTXC/PRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC clock cycle time	O		400±50 ppm		ns
MTXD/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL Output Setup time	T_{os}	Output Setup time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL	O	35	36	37	ns
MTXD/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL Output Hold time	T_{oh}	Output Hold time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL	O	3	4	5	ns
MRXD/PTXD[3:0], PHY2PTXD[3:0], MRXDV/PTXEN, PHY2PTXEN Setup time	T_s	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge setup time	I	4			ns
MRXD/PTXD[3:0], PHY2PTXD[3:0], MRXDV/PTXEN, PHY2PTXEN Hold time	T_h	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge hold time	I	2			ns
PHY Mode SNI Timing (DISINVERTER is pulled high)							
MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/PRXC, MRXC/PTXC clock cycle time	O		100±50 ppm		ns
MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Output Setup time	T_{os}	Output Setup time from MTXC/PRXC rising edge to MTXD[0]/PRXD[0], MTXEN/PRXDV, MCOL/PCOL	O	95	96	97	ns
MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Output Hold time	T_{oh}	Output Hold time from MTXC/PRXC rising edge to MTXD[0]/PRXD[0], MTXEN/PRXDV, MCOL/PCOL	O	3	4	5	ns
MRXD/PTXD[0], MRXDV/PTXEN Setup time	T_s	MRXD[0]/PTXD[0], MRXDV/PTXEN to MRXC/PTXC rising edge setup time	I	4			ns
MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Hold time	T_h	MTXD[0]/PRXD[0], MRXDV/PTXEN to MRXC/PTXC rising edge hold time	I	2			ns

Parameter	SYM	Condition	I/O	Min	Type	Max	Units
MAC Mode MII Timing (DISINVERTER is pulled low)							
100BaseT MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC clock cycle time	I		40±50 ppm		ns
10BaseT MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC clock cycle time	I		400±50 ppm		ns

Parameter	SYM	Condition	I/O	Min	Type	Max	Units
MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV Output Setup time	T_{os}	Output Setup time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV	O	22	24	26	ns
MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV Output Hold time	T_{oh}	Output Hold time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV	O	14	16	18	ns
MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN, MCOL/PCOL Setup time	T_s	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge setup time	I	4			ns
MRXD/PTXD, MRXDV/PTXEN, MCOL/PCOL Hold time	T_h	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge hold time	I	2			ns

Parameter	SYM	Condition	I/O	Min	Type	Max	Units
PHY Mode MII Timing (DISINVERTER is pulled low)							
100BaseT MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC clock cycle time	O		40±50 ppm		ns
10BaseT MTXC/PRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC clock cycle time	O		400±50 ppm		ns
MTXD/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL Output Setup time	T_{os}	Output Setup time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL	O	14	16	18	ns
MTXD/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL Output Hold time	T_{oh}	Output Hold time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL	O	22	24	26	ns
MRXD/PTXD[3:0], PHY2PTXD[3:0], MRXDV/PTXEN, PHY2PTXEN Setup time	T_s	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge setup time	I	4			ns
MRXD/PTXD[3:0], PHY2PTXD[3:0], MRXDV/PTXEN, PHY2PTXEN Hold time	T_h	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge hold time	I	2			ns
PHY Mode SNI Timing (DISINVERTER is pulled low)							
MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/PRXC, MRXC/PTXC clock cycle time	O		100±50 ppm		ns
MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Output Setup time	T_{os}	Output Setup time from MTXC/PRXC rising edge to MTXD[0]/PRXD[0], MTXEN/PRXDV, MCOL/PCOL	O	28	30	32	ns
MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Output Hold time	T_{oh}	Output Hold time from MTXC/PRXC rising edge to MTXD[0]/PRXD[0], MTXEN/PRXDV, MCOL/PCOL	O	68	70	72	ns

Parameter	SYM	Condition	I/O	Min	Type	Max	Units
MRXD/PTXD[0], MRXDV/PTXEN Setup time	T_s	MRXD[0]/PTXD[0], MRXDV/PTXEN to MRXC/PTXC rising edge setup time	I	4			ns
MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Hold time	T_h	MTXD[0]/PRXD[0], MRXDV/PTXEN to MRXC/PTXC rising edge hold time	I	2			ns

Parameter	SYM	Condition	I/O	Min	Type	Max
SMI Timing						
MDC	T_{CYC}	MDC clock cycle	40			ns
MDIO Setup Time	T_S	Write cycle	10			ns
MDIO Hold Time	T_H	Write cycle			10	ns
MDIO output delay relative to rising edge of MDC	T_{OV}	Read cycle			10	ns

9.6. Thermal Characteristics

Heat generated by the chip causes a temperature rise of the package. If the temperature of the chip (Tj, junction temperature) is beyond the design limits, there will be negative effects on operation and the life of the IC package. Heat dissipation, either through a heat sink or electrical fan, is necessary to provide a reasonable environment (Ta, ambient temperature) in a closed case. As power density increases, thermal management becomes more critical. A method to estimate the possible Ta is outlined below.

Thermal parameters are defined as below according to JEDEC standard JESD 51-2, 51-6:

1. θja (Thermal resistance from junction to ambient), represents resistance to heat flow from the chip to ambient air. This is an index of heat dissipation capability. A lower θja means better thermal performance.

   θja = (Tj - Ta) / Ph

   Where Tj is the junction temperature

   Ta is the ambient temperature

   Ph is the power dissipation

2. θjc (Thermal resistance from junction to case), represents resistance to heat flow from the chip to the package top case. θjc is important when an external heat sink is attached on the package top.

   θjc = (Tj - Tc) / Ph, where Tj is the junction temperature

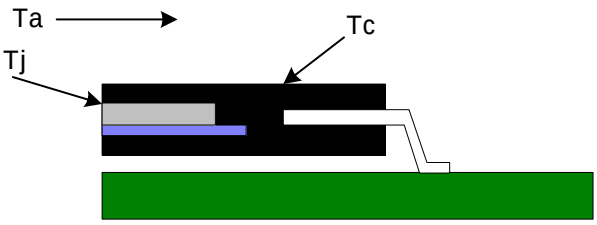


Figure 28. Cross-section of 128 PQFP

Table 54. Thermal Operating Range

Parameter	SYM	Condition	Min	Typical	Max	Units
Junction operating temperature	Tj		0	25	125	°C
Ambient operating temperature	Ta		0	25	70	°C

Table 55. Thermal Resistance

Parameter	SYM	Condition	Min	Typical	Max	Units
Thermal resistance: junction to ambient	θja	2 layer PCB, 0 ft/s airflow, ambient temperature 25°C		35.7		°C/W
Thermal resistance: junction to case	θjc	2 layer PCB, 0 ft/s airflow, ambient temperature 25°C		12.3		°C/W

** PCB conditions (JEDEC JESD51-7). Dimensions: 85 x 105 mm. Thickness: 1.6mm*

10. Application Information

10.1. UTP (10Base-T/100Base-TX) Application

In reviewing this material, please be advised that the center-tap on the primary side of the transformer must be left floating and should not be connected to ground through capacitors.

Vendor	Quad	Single
Pulse	H1164	H1102
Magnetic 1	ML164	ML102

Two types of transformers are generally used for the RTL8305SB Ver.D. One is a Quad (4-port) transformer with one common pin on both sides for an internal connected central tap. Another is a Single (1-port) transformer with two pins on both sides for a separate central tap.

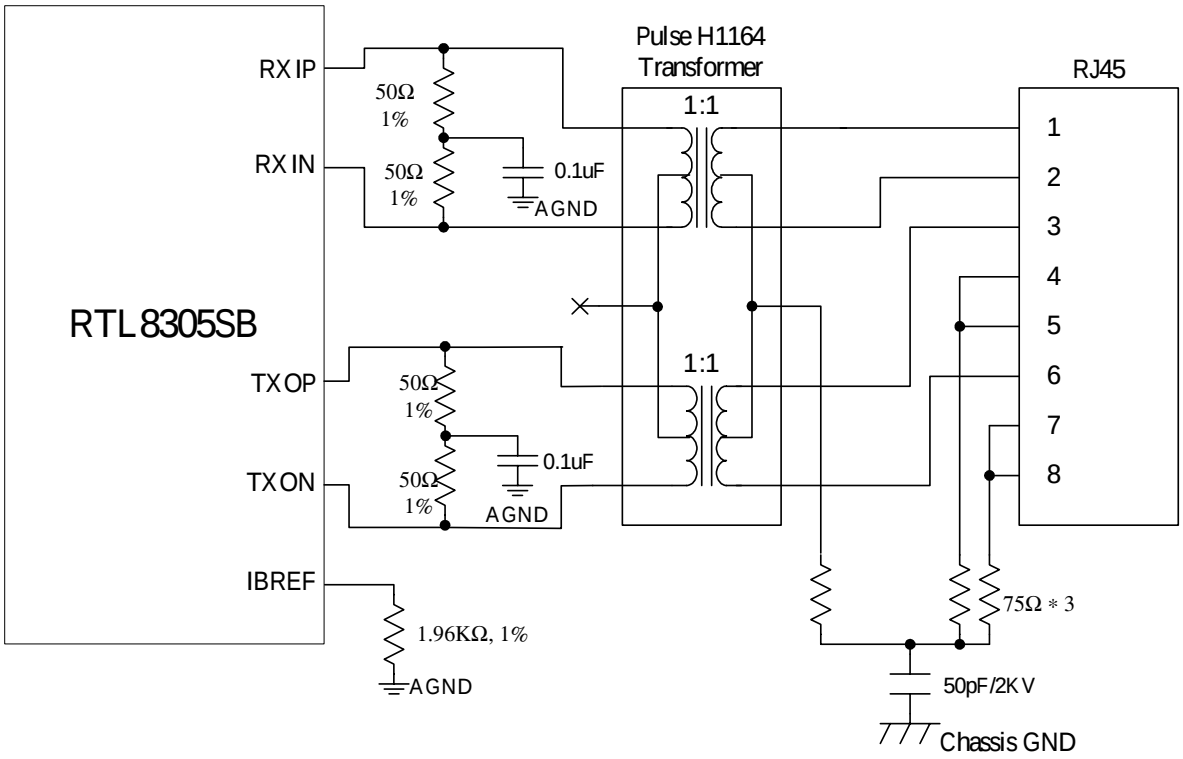


Figure 29. UTP Application for Transformer with Connected Central Tap

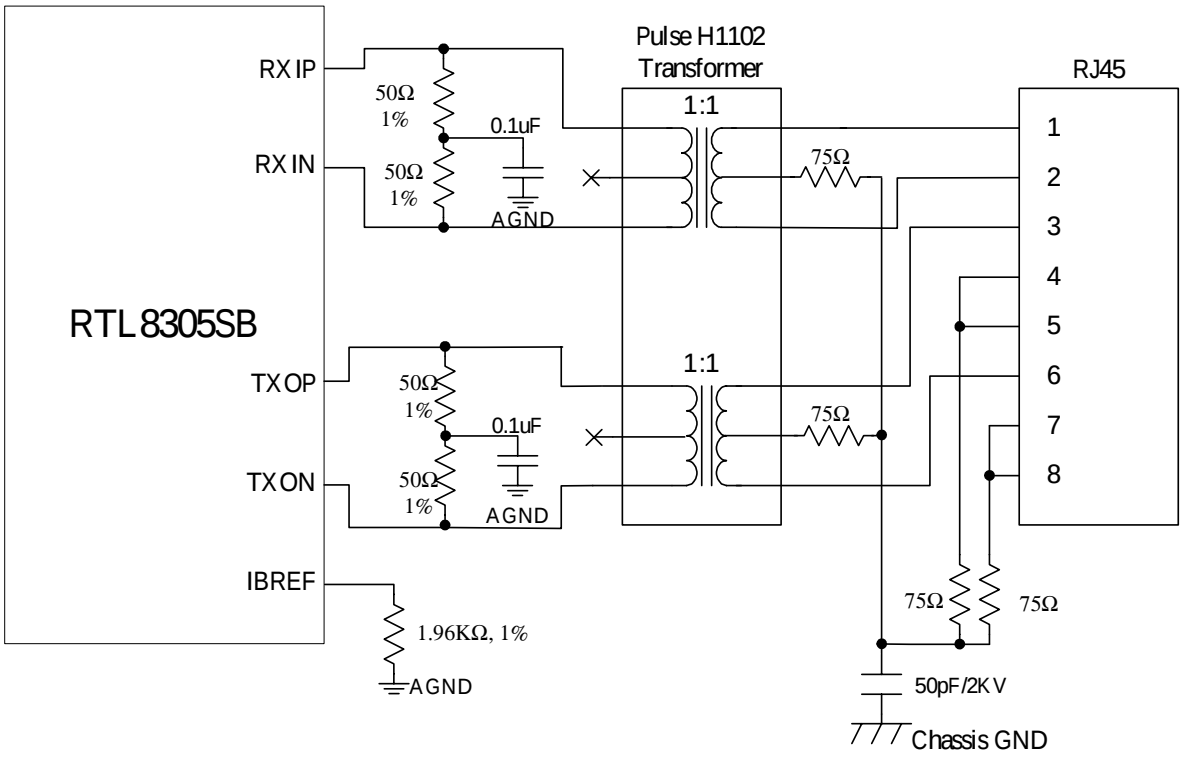


Figure 30. UTP Application for Transformer with Separate Central Tap

10.2. 100Base-FX Application

The following is an example of an RTL8305SB Ver.D connecting to a 3.3V fiber transceiver application circuit with a SIEMENS V23809-C8-C10 (3.3V~5V fiber transceiver, 1*9 SC Duplex Multimode 1300 nm LED Fast Ethernet/FDDI/ATM Optical Transceiver Module).

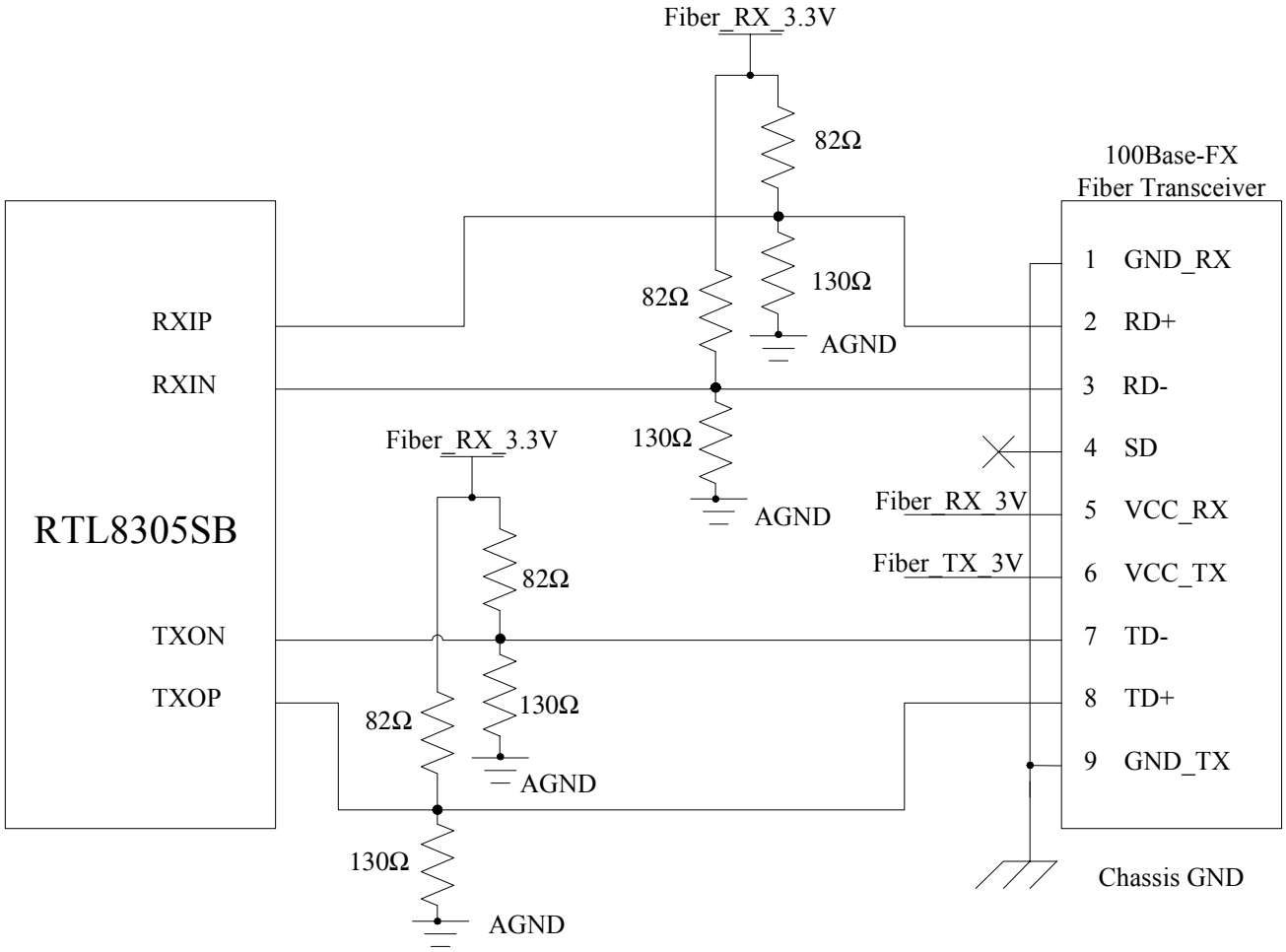


Figure 31. 100Base-FX with 3.3V Fiber Transceiver Application

The following is an example of an RTL8305SB Ver.D connected to a 5V fiber transceiver application circuit with a SIEMENS V23809-C8-C10 (3.3V~5V fiber transceiver, 1*9 SC Duplex Multimode 1300 nm LED Fast Ethernet/FDDI/ATM Optical Transceiver Module).

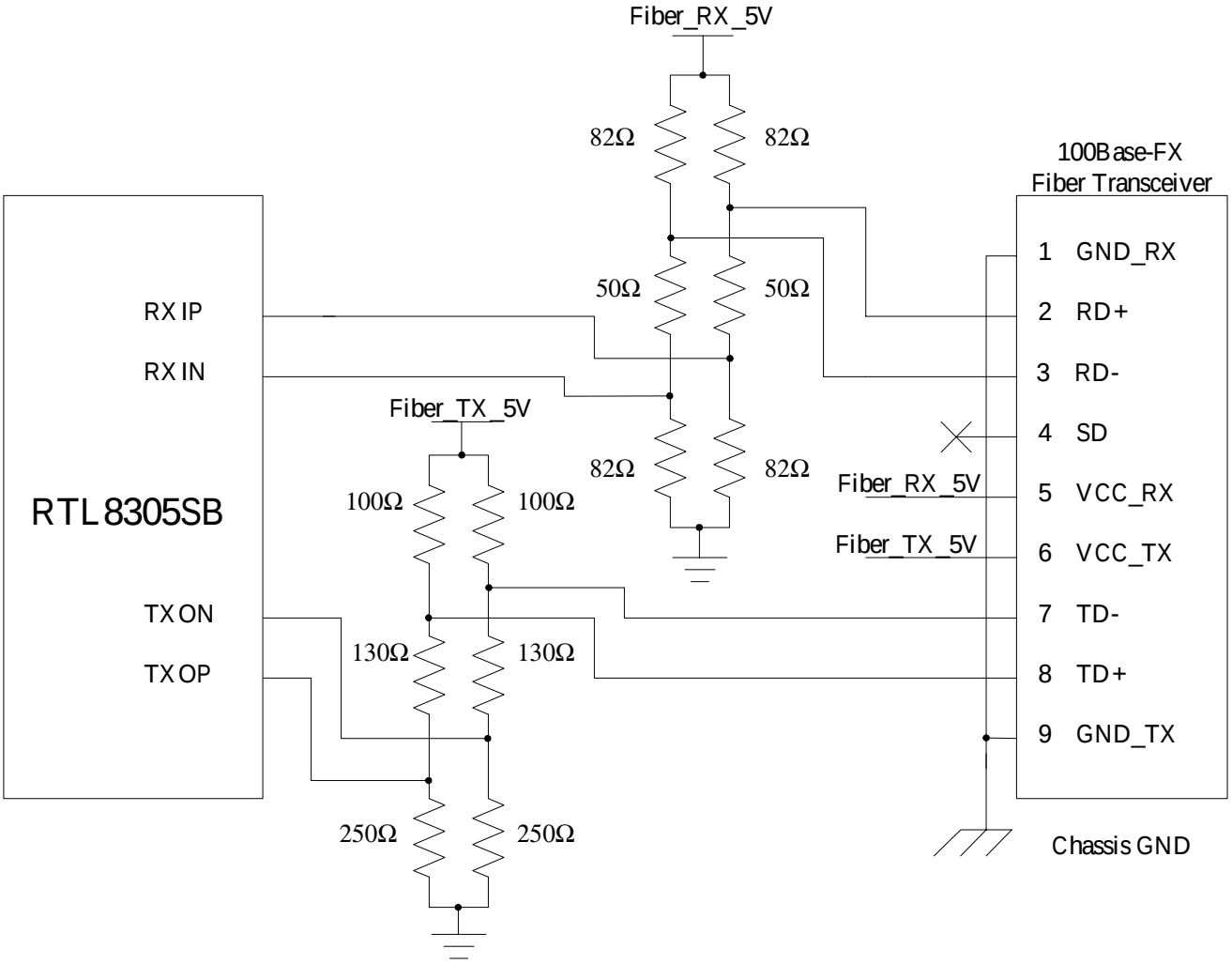


Figure 32. 100Base-FX with 5V Fiber Transceiver Application

11. System Application Diagrams

General System Application
1. General switch application
2. Router application:
3. HomePNA application
4. Other PHY application

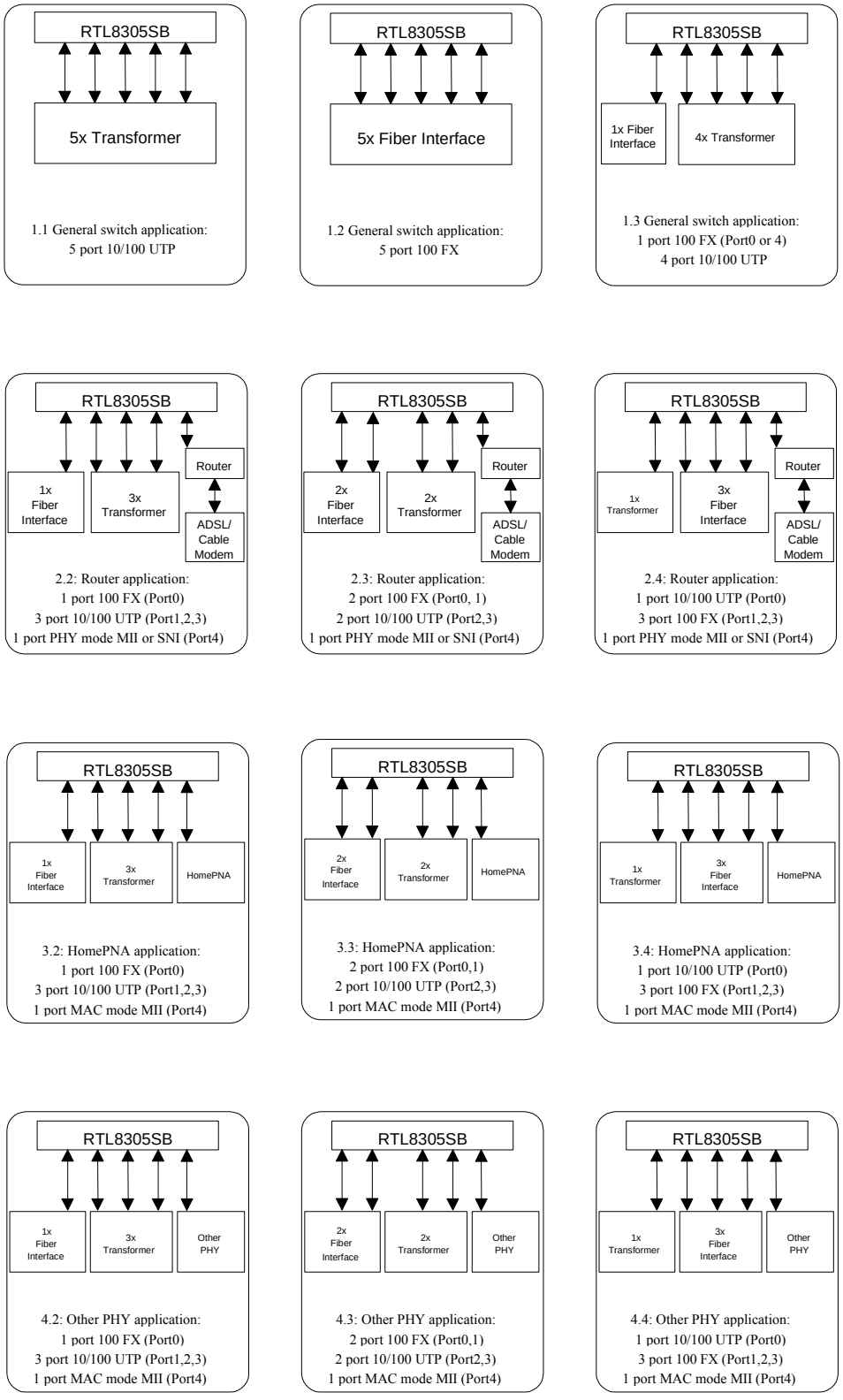


Figure 33. System Application Diagram

12. Design and Layout Guide

In order to achieve maximum performance using the RTL8305SB Ver.D, good design attention is required throughout the design and layout process. The following are some suggestions on recommendations to implement a high performance system.

General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<50mV).
- Verify the ability of critical components, e.g. clock source and transformer, to meet application requirements.
- Keep power and ground noise levels below 50mV.
- Use bulk capacitors (4.7μF-10μF) between the power and ground planes.
- Use 0.1μF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8305SB Ver.D chip.

Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other. Run orthogonal or separate by a ground plane.

Clock Circuit

- If possible, surround the clock by ground trace to minimize high-frequency emissions.
- Keep the crystal or oscillator as close to the RTL8305SB Ver.D as possible.

2.5V Power

- Do not connect a bead directly between the collector of the PNP transistor and RVDD. This will significantly affect the stability of the 2.5V power supply.
- Use a bulk capacitor (4.7μF-10μF) between the collector of the PNP transistor and the ground plane.
- Do not use one PNP transistor for more than one RTL8305SB Ver.D chip, even if the rating is enough.

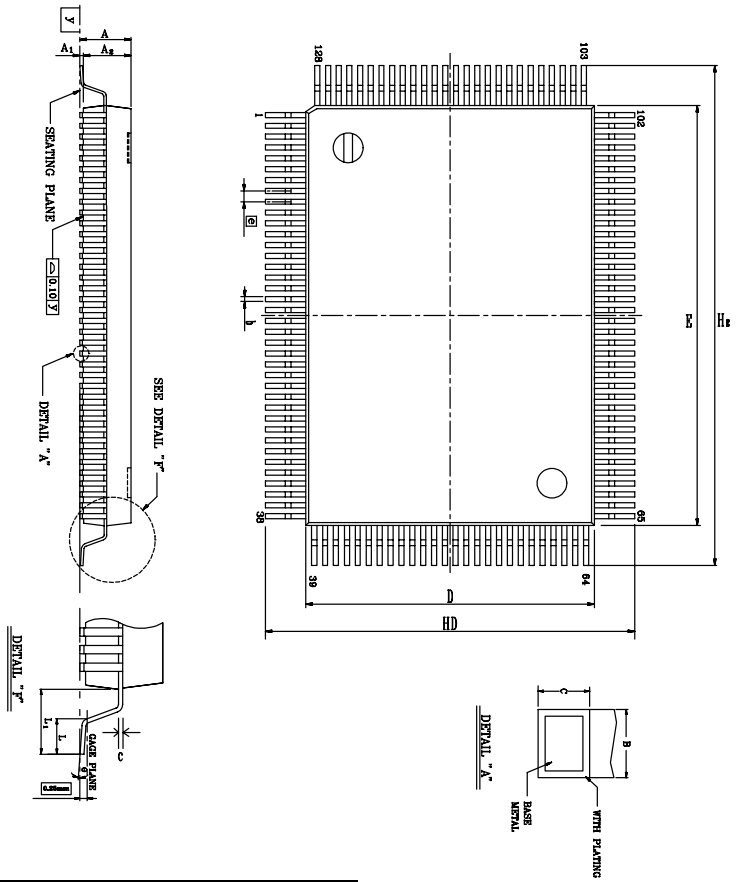
Power Plane

- Divide the power plane into 2.5V digital, 2.5V analog, and 3.3V analog.
- Use 0.1μF decoupling capacitors and bulk capacitors between each power plane and the ground plane.
- Power line connects from the source to the RTL8305SB Ver.D pin should be at least 10 mil wide.

Ground Plane

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.
- Ensure the chassis ground area is voided at some point such that no ground loop exists on the chassis ground area.

13. Mechanical Dimensions



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. Should be based on final visual inspection.

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